Optimal Control Strategy for Buck Converter Under Successive Load Current Change

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Abstract: A new control algorithm is presented for digitally controlled dc-dc converters to achieve a fast response under a successive load-change. Under the steady-state condition, the tight voltage regulation is processed by the conventional digital PID compensator. If the load disturbance is significant, the controller switches to an optimal control scheme. With the integration of the capacitor current, the proposed algorithm predicts the optimal switch over time based on the charge balance control, and the minimal voltage derivation and recovery time are thus achieved when the load current has a successive load-change. The method for calculating the optimal switch over time is described, and the implementation of the proposed algorithm with a digital controller is treated in detail. Furthermore, the simulation and experiment results are provided to validate the effectiveness of the approaches.

Key words: dc-dc converter; charge balance control (CBC); successive load-change; dynamic response

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1 Introduction

In modern dc-dc switch mode power supplies, the tight voltage regulation and fast response to load change are among the most important requirements[1]. A larger output filtering capacitor is always used to reduce output voltage derivation, however, this will occupies more board area and increase the cost. Thus, without modifying the hardware, couples of analog controllers and digital control algorithms have been developed in some previous literatures to improve the dynamic response of the dc-dc converters. Analog control strategies such as V^2 and hysteretic control, have received extensive attention in recent years, however, the main application challenge is the variations of the converter switching frequency[2-3]. Considering the intrinsic nonlinear nature of the switched regulators, various nonlinear methods have been introduced to achieve fast-transient responses to load-step events. In Ref.[4], the state plane of the dc-dc converter was partitioned by means of one or more switching surface, and a nonlinear sliding-mode controller was presented to drive the state trajectory rapidly converged to the regulation point. Since the selection of the switching surfaces is a central problem in the boundary-control theory, several design criteria and comparative studies regarding the choice of the switching surfaces have been proposed[5-6]. In Ref.[7], by using an 8-bit microcontroller, a self-regulating fuzzy control scheme was presented for the forward dc-dc converters. In Ref.[8], based on the Takagi-Sugeno model, the stability and performance was analyzed for the Boost converter which was controlled by a nonlinear fuzzy controller.

Although these approaches presented in the literatures differ with varying performance in terms of speed and robustness, they cannot

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achieve a faster response to load current disturbance. In Refs. [9, 10], some digital optimal schemes are discussed for dc-dc converters to approximate the fastest transient response during a transient event. In Ref. [11], by using the principle of capacitor charge balance control (CBC), a digital controller predicts the minimum voltage overshoot/undershoot and the recovery time for a buck converter. But it requires a sampling delay and complex mathematical computation. Based on the principle of CBC, couples of analog controllers and digital control algorithms were reported to improve the dynamic response of other power converters (such as the Boost converter, the Buck-Boost converter) in Refs. [12,13]. However, these controllers only considered one-step load current change, and the algorithm required the condition that load current should keep constant during a transient. Consequently, the CBC controller is unsuitable for a successive load-change.

A new digital control algorithm is discussed in this paper for dc-dc converters to enhance the dynamic performance during a successive load-change condition. Under a steady-state condition, the output voltage is tightly regulated by a digital voltage mode controller (VMC). Once the load current change is significant, an optimal control scheme is activated immediately. With the integration of the capacitor current, the proposed CBC algorithm predicts the switching time based on the charge balance control, and the optimal transient performance under a successive load-change is thus achieved. Compared with a conventional proportion integration differentiation (PID) controller, the proposed algorithm provides much better dynamic performance.

2 Principle of CBC Algorithm

The dc-dc Buck converter, composed of switchers Q_1, Q_2, an output filter circuit and a load R, is considered in this paper (Fig. 1).

According to the algorithm of capacitor charge balance, the average value of capacitor current over transient time must be equal to zero under one-step load current change [11].

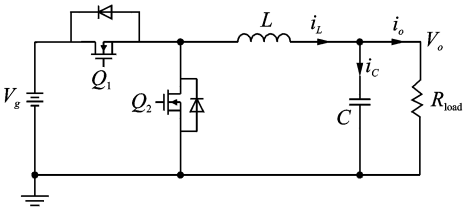


Fig. 1 SR-Buck converter

$$v_c(t_b) - v_c(t_a) = \frac{i_{cavg}}{C} = 0 \tag{1}$$

$$\frac{\int_{t_a}^{t_b} i_c(t)\,dt}{t_b - t_a} = 0 \tag{2}$$

where t_a, t_b are the beginning time and the end time of the transient period, respectively; i_c, v_c the current and the voltage of the output capacitor, respectively; C the value of the output capacitor. When Eq. (2) is satisfied, it means that the output voltage returns to the reference voltage after a transient period. Furthermore, if the inductor current i_L equals to the new load current at time t_b, the SR-Buck converter has recovered from a transient event (Fig. 2).

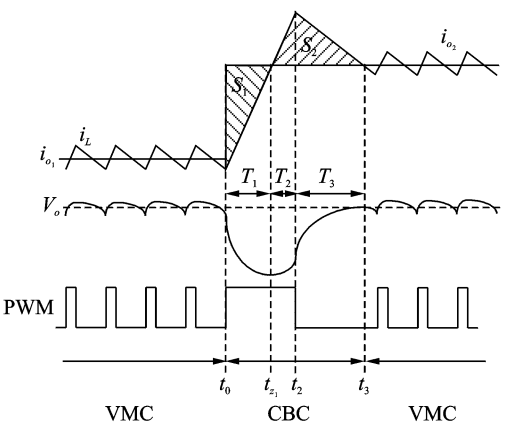


Fig. 2 Optimal dynamic response of Buck converter under positive load-current change

3 Mathematical Analysis of the Proposed Algorithm

In Fig. 2, the whole transient period under one-step load current change can be divided into two parts, i. e., one part that the capacitor supplies a portion of the load current before t_{z_1} and the other part that the capacitor begins recharge before t_3. In other words, the two parts determine the discharge portion (S_1) and the recharge portion (S_2). It should be noted that the capaci-

tor current crosses zero at t_{z_1}, which is regarded as the turning point in the transient period. Once t_{z_1} is obtained, the discharge portion of the capacitor can be calculated directly. Thus, the key point of the CBC algorithm is to accurately obtain the value T_1 (determined by t_{z_1}), therefore, the charge of the capacitor keeps balance at the end of a transient period.

Before the introduction of the proposed algorithm, some assumptions should be considered, that is,

(1) the ESR and ESL can be neglected;

(2) the values of the inductor and capacitor keep constant;

(3) the input voltage keeps unchanged during the transient.

3.1 One-step load-current change

Firstly, the rising and falling slew rate of the inductor current is given as

$$\frac{\mathrm{d}i_L}{\mathrm{d}t}\Big|_{\text{rising}}=\frac{V_g-V_o}{L}=m_1 \tag{3}$$

$$\frac{\mathrm{d}i_L}{\mathrm{d}t}\Big|_{\text{falling}}=-\frac{V_o}{L}=-m_2 \tag{4}$$

Based on Fig. 2, the discharge portion S_1 can be calculated as

$$S_1=\int_{t_0}^{t_{z_1}} i_c(t)\,\mathrm{d}t \tag{5}$$

while the charge portion S_2 can be given as

$$S_2=\int_{t_{z_1}}^{t_2} i_c(t)\,\mathrm{d}t+\int_{t_2}^{t_3} i_c(t)\,\mathrm{d}t=\int_{t_{z_1}}^{t_2} i_c(t)\,\mathrm{d}t+\frac{m_1}{m_2}\int_{t_{z_1}}^{t_2} i_c(t)\,\mathrm{d}t=\left(1+\frac{m_1}{m_2}\right)\int_{t_{z_1}}^{t_2} i_c(t)\,\mathrm{d}t=\frac{V_g}{V_o}\int_{t_{z_1}}^{t_2} i_c(t)\,\mathrm{d}t \tag{6}$$

According to the principle of the CBC, at the end of transient, the following equations should be fulfilled

$$S_1+S_2=0 \tag{7}$$

$$V_o\int_{t_0}^{t_{z_1}} i_c(t)\,\mathrm{d}t+V_g\int_{t_{z_1}}^{t_2} i_c(t)\,\mathrm{d}t=0 \tag{8}$$

Thus, the optimal transient time T_1, T_2 and T_3 can be given by

$$T_1=t_{z_1}-t_0,\ T_2=t_2-t_{z_1},\ T_3=\frac{m_1}{m_2}T_2 \tag{9}$$

A similar analysis can be performed for a negative load step based on Fig. 3. The following equations should be satisfied

$$S_1+S_2=0 \tag{10}$$

$$(V_g-V_o)\int_{t_0}^{t_{z_1}} i_c(t)\,\mathrm{d}t+V_g\int_{t_{z_1}}^{t_2} i_c(t)\,\mathrm{d}t=0 \tag{11}$$

Moreover, the optimal transient time T_1, T_2 and T_3 under a negative load step change can be obtained

$$T_1=t_{z_1}-t_0,\ T_2=t_2-t_{z_1},\ T_3=\frac{m_2}{m_1}T_2 \tag{12}$$

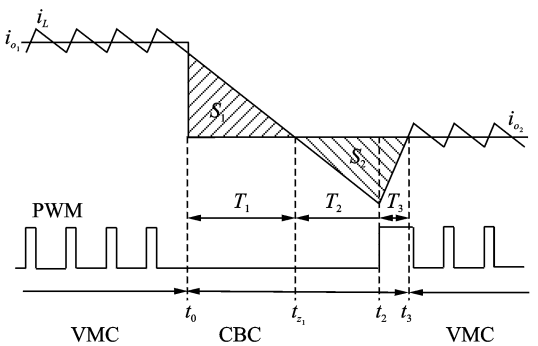


Fig. 3 Optimal dynamic response of Buck converter under negative load-current change

3.2 Successive load-current change

If a successive positive load-current change is considered, the proposed algorithm executes the corresponding action according to the different step change, as shown in Figs. 4 (a, b). It is obvious that the response is more complicate than that of the one-step load change. It is divided into several parts, including the discharge portion (S_1, S_3) and the recharge portion (S_2, S_4) in Fig. 4. However, the detection of the point (t_{z_1} and t_{z_2}) is still the key step in the proposed algorithm, because the capacitor turns into the recharge portion at t_{z_1} and t_{z_2}.

According to the algorithm of the capacitor charge balance control, at the end of transient, the following equation should be fulfilled

$$S_1+S_2+S_3+S_4=0 \tag{13}$$

It should be noted that the recharge portion S_4 can be calculated similarly to the one-step load change

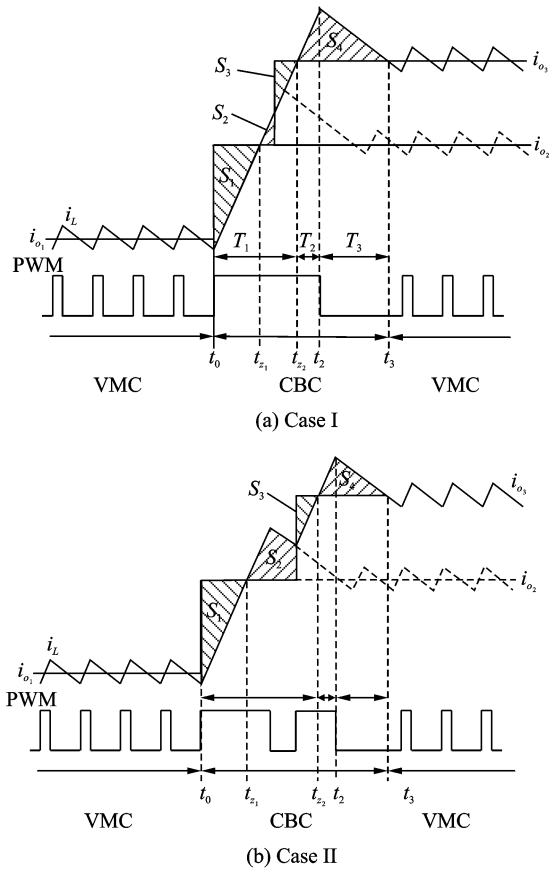


Fig. 4 Optimal dynamic response of Buck converter under successive positive load current change

$$S_4=\int_{t_{z_2}}^{t_2} i_c(t)\,\mathrm{d}t+\int_{t_2}^{t_3} i_c(t)\,\mathrm{d}t=\int_{t_{z_2}}^{t_2} i_c(t)\,\mathrm{d}t+\frac{m_1}{m_2}\int_{t_{z_2}}^{t_2} i_c(t)\,\mathrm{d}t=\left(1+\frac{m_1}{m_2}\right)\int_{t_{z_2}}^{t_2} i_c(t)\,\mathrm{d}t=\frac{V_g}{V_o}\int_{t_{z_2}}^{t_2} i_c(t)\,\mathrm{d}t \tag{14}$$

Moreover, the sum of the portions S_1, S_2, S_3 can be given directly by the integration of the capacitor current over the period $[t_0 \quad t_{z_2}]$

$$S_1+S_2+S_3=\int_{t_0}^{t_{z_2}} i_c(t)\,\mathrm{d}t \tag{15}$$

Substituting Eqs. (14, 15) into Eq. (13) yields

$$\int_{t_0}^{t_{z_2}} i_c(t)\,\mathrm{d}t+\frac{V_g}{V_o}\int_{t_{z_2}}^{t_2} i_c(t)\,\mathrm{d}t=0\Rightarrow V_o\int_{t_0}^{t_{z_2}} i_c(t)\,\mathrm{d}t+V_g\int_{t_{z_2}}^{t_2} i_c(t)\,\mathrm{d}t=0 \tag{16}$$

In Fig. 5, the optimal transient time T_1, T_2 and T_3 can be calculated as

$$T_1=t_{z_2}-t_0,\ T_2=t_2-t_{z_2},\ T_3=\frac{m_1}{m_2}T_2 \tag{17}$$

A similar analysis can be carried out for a negative load step based on Fig. 5. The following equation should be fulfilled

$$(V_g-V_o)\int_{t_0}^{t_{z_2}} i_c(t)\,\mathrm{d}t+V_g\int_{t_{z_2}}^{t_2} i_c(t)\,\mathrm{d}t=0 \tag{18}$$

Then the optimal transient time has the following expression

$$T_1=t_{z_2}-t_0,\ T_2=t_2-t_{z_2},\ T_3=\frac{m_2}{m_1}T_2 \tag{19}$$

With some minor change to Eqs. (16—19), the same analysis can be applied to the dc-dc converter under other successive load change conditions, which will not be discussed in this paper.

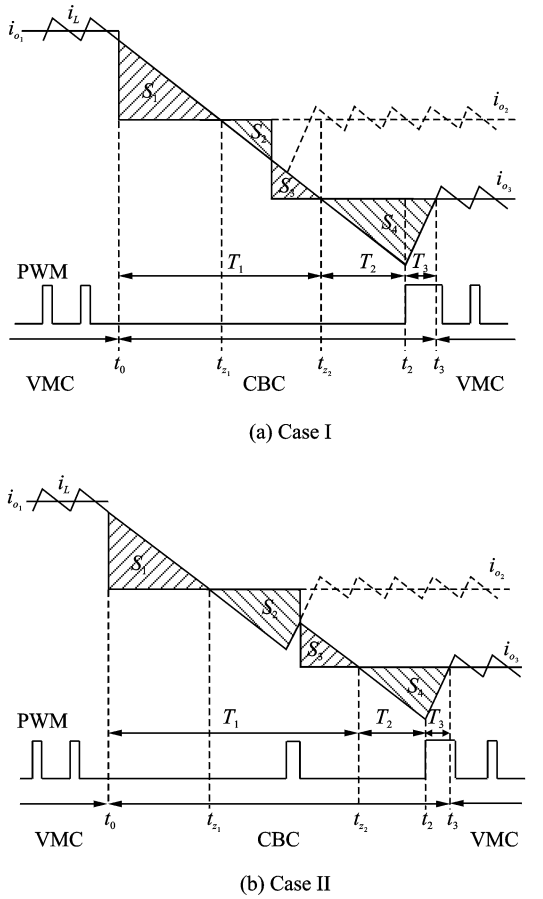


Fig. 5 Optimal dynamic response of Buck converter under a successive negative load current change

4 Implementation of the Proposed Digital Controller

4.1 Outline of algorithm operation

According to the analysis in Section 3, the key steps of the proposed algorithm can be listed as follows:

(1) After detecting a load current change (by comparing the change of the load current i_o with the predefined threshold), the optimal control

scheme is activated immediately at t_0, and the counter and the integration of the capacitor current i_c in the digital controller are triggered;

(2) The duty cycle is set as the maximum value 100% (a positive step change) or the minimum value 0% (a negative step change), which drives the induct current i_L rise or fall at its maximum slew rate;

(3) Once Eq. (8) or Eq. (11) is fulfilled, which means i_L reaches its peak value or valley value (at t_2 in Figs. 2, 3), the duty cycle is set to 0% (a positive step change) or 100% (a negative step change);

(4) If a successive load change occurs (by comparing the i_o change with the threshold), the duty cycle is reset as 100% or 0% again, as shown in Figs. 4,5;

(5) When the condition of the charge balance control is satisfied, the digital controller returns to the conventional digital PID control scheme again.

4.2 Hardware implementation

The hardware implementation diagram of the proposed charge balance control algorithms is shown in Fig. 6. R_L and R_o are the high precision resistances used to sample the inductor current and the load current. C_{v_sens}, C_{iL_sens} and C_{io_sens} are the decoupling capacitor of the operational amplifiers.

4.3 Digital controller based on FPGA

In Fig. 7, the proposed algorithm is programmed by Block diagram method in FPGA, with the logic elements (4, 429), registers (2,848) and memory bits (251,560).

In Fig. 7, the clock module products the clock signals, which are used in other modules and A/D sample. The digital PID module is constructed according to the following equation

$$d(k)=d(k-1)+Ae(k)+Be(k-1)+Ce(k-2) \tag{20}$$

where the coefficients are given as

$$A=K_p+\frac{T}{\tau_i}+\frac{\tau_d}{T},\ B=-K_p-\frac{2\tau_d}{T},\ C=\frac{\tau_d}{T} \tag{21}$$

where K_p, τ_i, τ_d are the parameters of the PID controller. T is the sample period.

The proposed algorithm is programmed in the CBC module, including several submodules, such as the load step detection, the crossing-zero judgment of the i_c, and the charge balance control (Fig. 7).

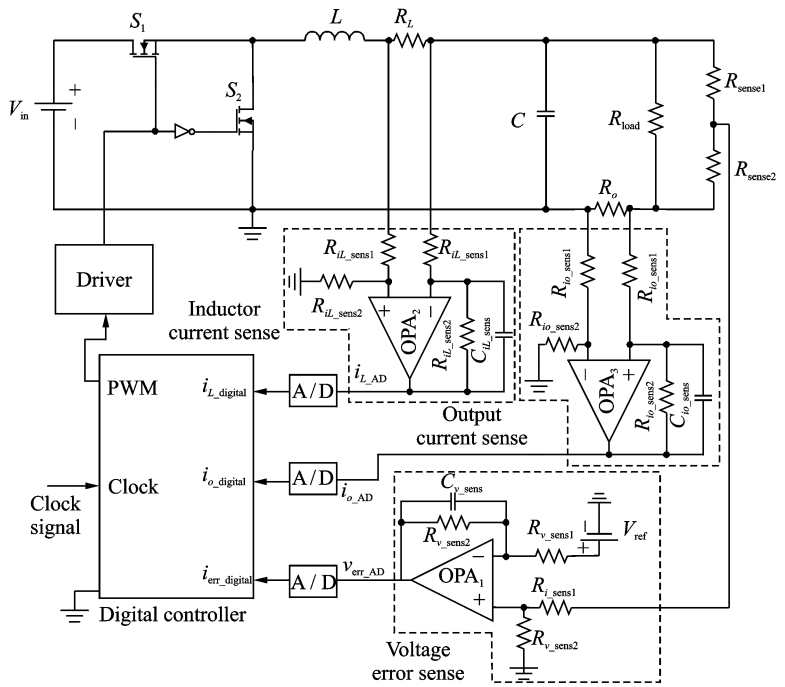


Fig. 6 Hardware implementation diagram

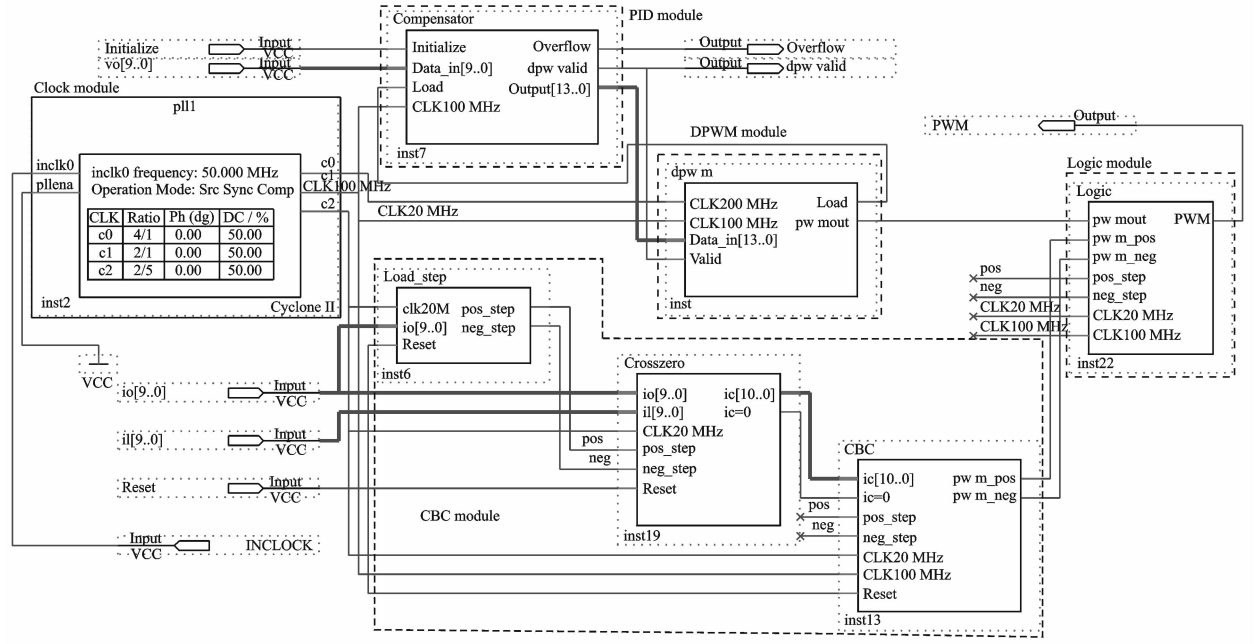


Fig. 7 Block diagram implementation of the proposed algorithms in FPGA

5 Simulation and Experiment Results

To verify the performance of the proposed method, a Buck converter, undergoing several successive load current changes, was proposed. The parameters of the converter were provided as follows: $V_{in}=5$ V, $V_o=1.5$ V, $f_s=250$ kHz, $L=1.5$ μH, $C=290$ μF.

5.1 Simulation results

Simulation is performed by Matlab/Simulink. For comparison, a well-designed digital PID controller with bandwidth of 30 kHz and phase margin of 52° is also simulated.

$$d(k)=d(k-1)+27.8e(k)-49.54e(k-1)+22.1e(k-2) \quad (22)$$

Fig. 8 illustrates the different dynamic performance of the Buck converter under a PID controller and a CBC controller, while a positive successive load step change (from 0 A to 5 A to 10 A). It is observed that, by using the PID controller, the undershoot of the output voltage is 102 mV and the recovery time is 81 μs; while using the proposed CBC algorithm, the overshoot is reduced to 15 mV and the settling time is reduced to 11 μs, which are improved by 85% and 86%, respectively, compared with those of the PID controlled converter.

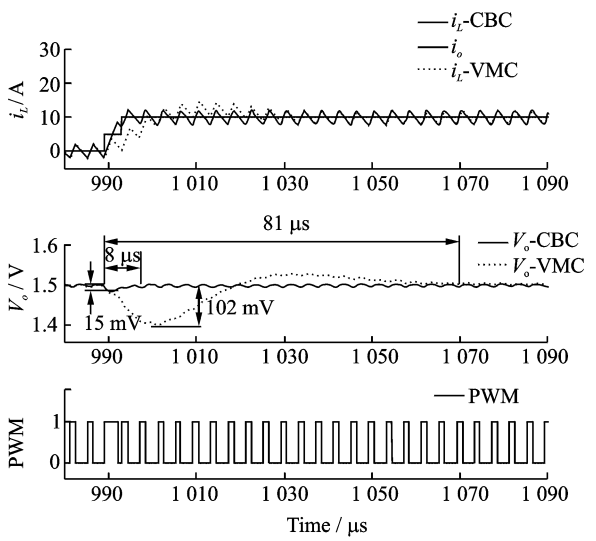


Fig. 8 Simulation results of output voltage response to a positive successive load current change (0 A→5 A→10 A)

For a negative successive load step change (from 10 A to 5 A to 0A), as shown in Fig. 9, with the proposed controller, the overshoot is reduced to 21 mV, which is improved by 76%, and the settling time is reduced to 12 μs, which is improved by 84%, compared with those of the PID controlled converter.

Simulation results demonstrated that the settling time of the converter with the proposed algorithm is improved significantly compared to that of the PID controlled converter.

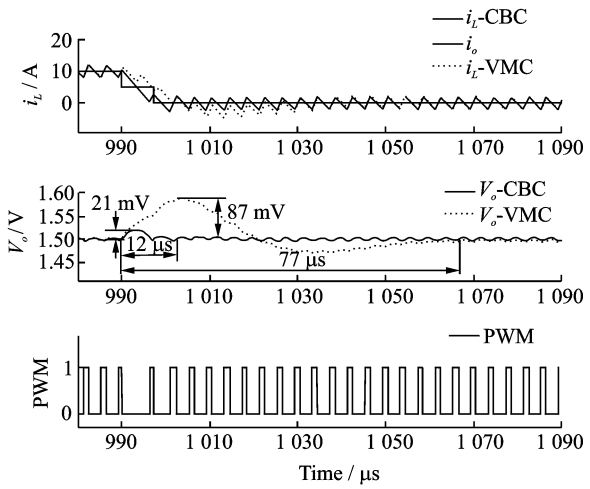
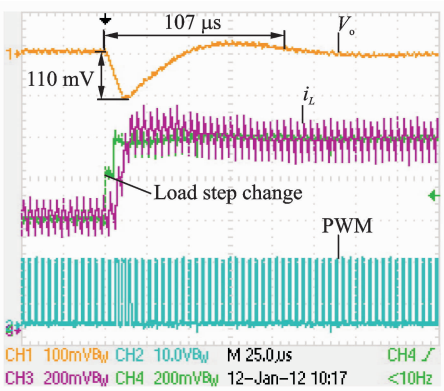


Fig. 9 Simulation results of output voltage response to an negative successive load current change (10 A→5 A→0 A)

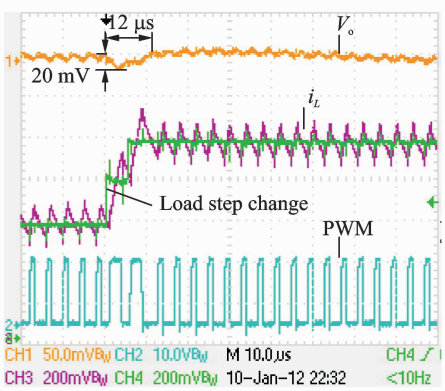
5.2 Experimental results

An experimental prototype of a Buck converter was designed and implemented with FPGA by using the aforementioned algorithm.

In Fig. 10(a) and Fig. 11(a), the experimental results illustrate the transient performance of the PID controller under the successive load step change between 0 A and 10 A. Limited by the bandwidth, the voltage mode controller has large voltage variations and long recovery time. For a positive load transient, the undershoot voltage is about 110 mV with 107 μs settling time. While, the overshoot voltage is 120 mV with 118 μs settling time during a negative load transient.

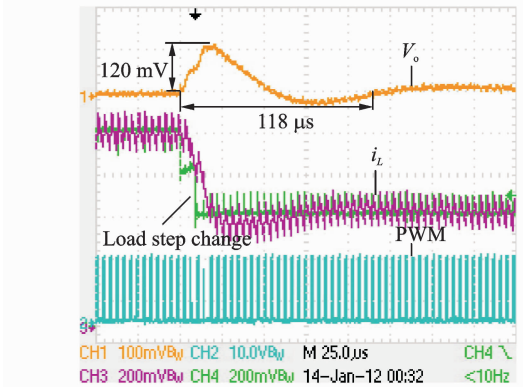


(a) Experimental results using the PID controller

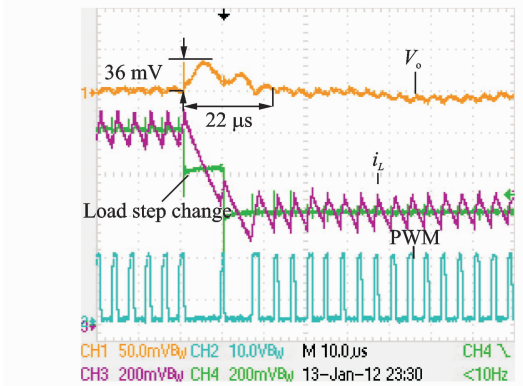


(b) Experimental results using the CBC controller

Fig. 10 Experimental results of successive positive load transient case 0 A→5 A→10 A



(a) Experimental results using the PID controller



(b) Experimental results using the CBC controller

Fig. 11 Experimental results of successive negative load transient case 10 A→5 A→0 A

Experimental results of the proposed CBC controller under the load step change between 10 A and 0 A are shown in Fig. 10(b) and Fig. 11(b). Compared to the PID controller, the undershoot voltage is reduced by 81% with the recovery time shortened by 88% for a positive load step change, while the overshoot voltage is reduced by 70% with the recovery time shortened by 81% for a negative load step change.

6 Conclusions

A practical digital control algorithm has been

presented for improving the dynamic performance of dc-dc converters under a successive load-change condition. The controller utilizes the principle of the charge balance control, where a PID compensator and a CBC controller are combined to provide the tight output voltage regulation and fast transient response. Furthermore, conditions and equations for capacitor charge balance are derived. The effectiveness of the proposed algorithm is verified on an experimental prototype of a Buck converter, demonstrating stable operation and fast transient response in different operating conditions.

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