A 60 GHz Phased Array System Analysis and Its Phase Shifter in a 40 nm CMOS Technology

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Abstract: A 60 GHz phased array system for mm-wave frequency in 5G is introduced and a 5 bit digitally controlled phase shifter in 40 nm CMOS technology is presented. In a phased array system, the signal to noise ratio (SNR) of the receiver is improved with the beaming forming function. Therefore, the communication data rate and distance are improved accordingly. The phase shifter is the key component for achieving the beam forming function, and its resolution and power consumption are also very critical. In the second half of this paper, an analysis of phase shifter is introduced, and a 60 GHz 5 bit digitally controlled phase shifter in 40 nm complementary metal oxide semiconductor (CMOS) technology is presented. In this presented phase shifter, a hybrid structure is implemented for its advantage on lower phase deviation while keeping comparable loss. Meanwhile, this digitally controlled phase shifter is much more compact than other works. For all 32 states, the minimum phase error is 1.5°, and the maximum phase error is 6.8°. The measured insertion loss is -20.9 ± 1 dB including pad loss at 60 GHz and the return loss is more than 10 dB over 57—64 GHz. The total chip size is 0.24 mm^2 with 0 mW DC power consumption.

Key words: 5G; 60 GHz; complementary metal oxide semiconductor (CMOS); millimeter wave; phased array; phase shifter

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0 Introduction

For the last decades, the long term evolution (LTE) enhancements, such as advanced multiple-input-multiple-output (MIMO), coordinated multi-point (CoMP), heterogeneous networks (HetNets), and carrier aggregation (CA), can no longer keep pace with the needs of capacity from the rocketing increase of data. The bandwidth-intensive immersive media services like virtual reality (VR), augmented reality (AR), vehicle-to-everything (V2X) and internet of things (IoT), which were earlier confined to wired transmission, are now making a foray into mobile and indoor wireless devices. Full high definition (Full HD) video, ultra HD (UHD) video, 3D video, wireless HDMI video streaming, and other wireless displays are also being rapidly shared and spread through social mobile applications and indoor wireless applications. This leads the telecommunication industry and academia to spend significant amounts of research efforts in the fifth generation (5G) and the sixth generation (6G) to provide higher data rates, lower latency and improved robustness for solving the demands of data transfer [1-5].

At millimeter wave (mm-Wave) bands, the signal is transmitted from 30 GHz to 300 GHz with a wavelength of 10 mm and 1 mm, respectively. The high carrier frequency brings wide signal bandwidth and thus increases the data rate of wireless communication. Also, short wavelength means the antennas used to transmit and receive signals can be smaller, allowing the highly compact active phased array. WRC-191 Agenda 1.13 published by the Federal Communications Commission (FCC) in 2016 is shown in Table 1, where frequency spec-

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Table 1 Spectrum in 5G from FCC

Band identifier/GHz	Frequency range/GHz	Bandwidth/MHz	Channelization	Licensed
28	27.50—28.35	850	2×425 MHz unpaired blocks	Yes
37	37.00—38.60	1 600	8×200 MHz unpaired blocks	Yes
39	38.60—40.00	1 400	7×200 MHz unpaired blocks	Yes
64—71	64.00—71.00	7 040	4×1 760 MHz unpaired blocks	No

trum bands 28—30 GHz, 38—40 GHz, and 64—71 GHz are allocated. While the bands 28—30 GHz and 38—40 GHz are recommended as outdoor mm-wave base stations (BSs), 60 GHz frequency band has emerged as the most promising candidate for indoor high-speed communications. In addition, IEEE 802.11ad Standard was formed[3,6], and the unlicensed spectrum worldwide at 60 GHz has a maximum bandwidth of 9 GHz from 57 GHz to 66 GHz in Europe, with four sub-channels and one sub-channel bandwidth of 2.16 GHz, as shown in Table 2. In general, this band has the superiority in the aspects of speeds of multi-Gb/s, low latency for control of real-time applications, extremely robust communication paths for critical services as well as small cell-centric with ease of installation and planning.

Table 2 60 GHz frequency spectrum in the 802.11ad Standard

Region	Lower frequency/GHz	Upper frequency/GHz	Usable channels
UAS	57.05	71.00	1,2,3,4,5,6
Canada	57.05	64.00	1,2,3
South Korea	57.00	64.00	1,2,3
EU	57.00	66.00	1,2,3,4
Japan	57.00	66.00	1,2,3,4
Australia	57.00	66.00	1,2,3,4
China	59.00	64.00	2,4

In this paper, a 60 GHz mm-wave phased array system is introduced, especially a comparison of different phased array architectures. A system budget estimation is provided. Then the phase shifter is analyzed and its design consideration is shown. A passive phase shifter in 40 nm CMOS technology is presented and at last the conclusions are drawn.

1 mm-Wave Phased Arrays System

1.1 Introduction of phased arrays

A typical phased array receiver (RX) consists of multiple signal paths with an antenna and a delay block on each path. A power combiner later combines the signal power on each path, as shown in Fig.1. Because of different path distances, the signals on each path arrive at the corresponding antenna at different time. The antenna elements of the array are assumed to be a one-dimensional n-element uniform linear array (ULA). The path difference ($\triangle d$) is defined as

$$\triangle d = d\sin\theta = c\tau = \frac{\triangle\varphi}{2\pi} * \lambda \tag{1}$$

where d is the distance between antenna elements, θ the angle of incidence, c the speed of light, λ the wavelength, τ and $\triangle\varphi$ denote the time difference and phase difference of different signal paths, respectively. As stated from Eq.(1), the path delay could be implemented by either time delay or phase delay. With the delay blocks at different paths, the signals from the desired angle are aligned coherently, so they could be added in phase by the power combiner while signals from undesired angles are added incoherently. Noises are canceled out since they are modeled as random signals.

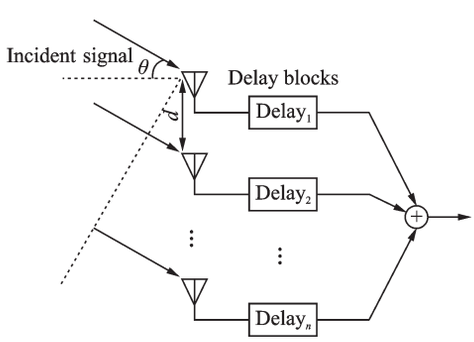

Fig.1 Generic delay array architecture

Such array behavior has the advantage of significant attenuation of incident interference from other angles. The beam pattern of a 16-element ULA antenna array is illustrated in Fig.2 with beam steering to 30° and an antenna spacing of $\lambda/2$. According to

Fig.2, signals from the desired angle (30°) are added up coherently while signals from other angles are significantly suppressed.

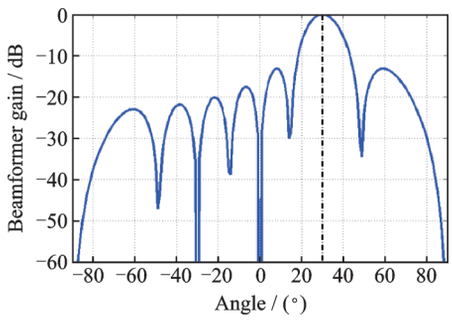

Fig.2 Beam pattern of a 30° incident signal

Another benefit of using phased arrays is the signal to noise ratio (SNR) enhancement at the output of the phased array receiver compared with the single element receiver. Signal power from desired angle adds coherently and power from undesired angle cancels out under the assumption that an ideal n-element phased array with unit antenna gain G_{ant} and perfect isolation between antenna elements. However, considering the problem of antenna coupling or LO phase noise generated from LO phase shifting which introduces correlation of noise sources, the SNR improvement is degraded.

$$F_{\text{RX}} = \frac{n \cdot \text{SNR}_{\text{in,single-element}}}{\text{SNR}_{\text{out,array}}} = n \cdot F_{1:n} \tag{2}$$

where $F_{1:n}$ refers to the noise factor of an n-element phased array RX when a single element input is taken with respect to an n-element output, as

$$F_{1:n} = \frac{\text{SNR}_{\text{in,single-element}}}{\text{SNR}_{\text{out,array}}} \tag{3}$$

Assuming that the noise is dominated by the noise of front-end F_{FE} of each path, and ignoring other receiver components as

$$F_{1:n} = \frac{F_{\text{FE}}}{n} \tag{4}$$

SNR at the output is close to but less than n times of SNR at the output of each front end and the noise factor of a phased array RX is close to but larger than the noise factor of each front end. Assuming a parameter η ($\eta \leqslant 1$) denoting effects such as antenna coupling and influence of other RX components, the noise factor of array RX could be denoted as

$$F_{\text{RX}} = \frac{n \cdot \text{SNR}_{\text{in,single-element}}}{n \cdot \eta \cdot \text{SNR}_{\text{out,FE}}} = \frac{F_{\text{FE}}}{\eta} \tag{5}$$

While the output array SNR is shown as

$$\text{SNR}_{\text{out,array}} = n \cdot \eta \cdot \text{SNR}_{\text{out,FE}} \tag{6}$$

According to these equations, the phased array receiver could be considered equivalent to a single element receiver with noise factor F_{RX} and antenna gain $n \cdot G_{\text{ant}}$. The SNR enhancement enables the phased array RX to achieve better sensitivity compared to single element RX.

1.2 Architecture comparison

There are four locations suitable for the phase shifter to achieve the phase shifting function. Those are in the RF path, in the LO path, in the IF path, or in the digital domain.

The architecture of phase shifter implemented in the digital domain is shown in Fig.3. In this architecture, the phase shifting is implemented in the digital baseband. Phase shifting in the digital domain has the advantage of flexibility and accuracy. However, it also requires the RF/IF part on each signal path, including mixer, analog-to-digital converter (ADC), resulting in a large area and higher power consumption. Besides, interference signals are canceled out only after phase shifting, and all circuit blocks need a large dynamic range to process these interferers without degrading the signal of interest, which increases the complexity of RF and ADC blocks and power consumption. The large IF bandwidth of 60 GHz and high data rate also make the digital approach an expensive solution. Therefore, typically phase shifting of 60 GHz signals takes place at RF/LO/IF path before the ADC block, with their pros and cons, respectively.

The RF phase shifter based architecture is shown in Fig.4. In this architecture, the signal combining and phase shifting are carried out at RF path[7-9]. The LNA and phase shifter composes an RF front-end on each antenna path, and other radio blocks are shared, resulting in reduced area and power consumption. Additionally, since interference signals are canceled after power combining, both noise figure and linearity requirements of fol-

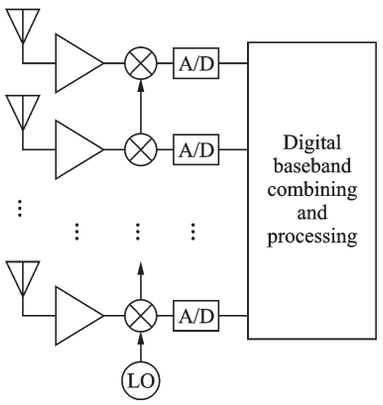

Fig.3 Simplified digital phase shifting

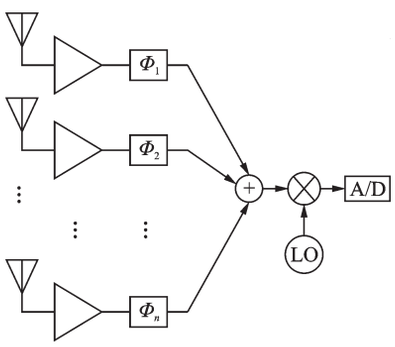

Fig.4 Simplified scheme of phase shifting at RF path

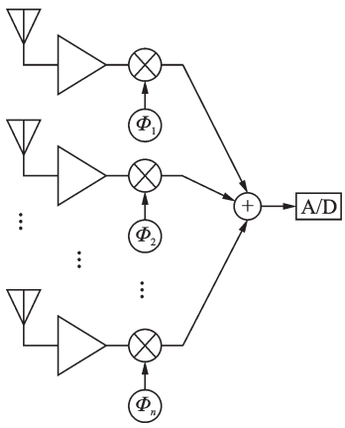

Fig.5 Simplified scheme of phase shifting at LO path

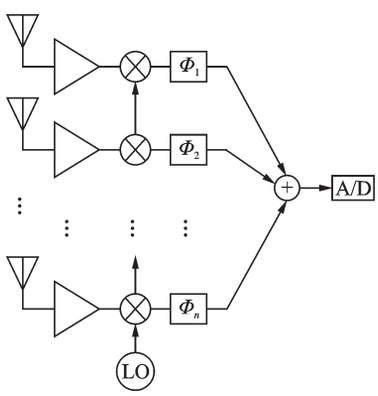

Fig.6 Simplified scheme of phase shifting at IF path

lowing blocks are relaxed, allowing compensation for other system requirements such as power consumption. However, the phase shifting at RF introduces losses on RF signals, which affects the receiver sensitivity and quality of the received signal.

The LO phase shifter based architecture is shown in Fig.5. In this architecture, phase shifting is presented at the LO path and power combined at IF. Phase shifting at LO path[10-11] is advantageous in which the loss of phase shifter does not directly deteriorate the receiver sensitivity, but affected by the LO phase noise instead. Besides, the power is combined at IF which is easier to implement, but requires multiplication of more circuits and needs to deal with clock distribution issue. Since interferers are not canceled before mixer, the dynamic range requirement of the mixer is strengthened.

The IF phase shifter based architecture is shown in Fig.6. In this architecture, the phase shifting and power combining are carried out at the IF path, which require a relatively broadband phase shifter (compared to the center frequency). For the passive high pass and low pass passive phase shifter, to achieve a certain phase shift, its inductor and capacitor values are inversely proportional to the carrier frequency. Since the values of integrated passive components are directly related to their physical size, passive phase shifters at IF consume a larger area compared with the ones at RF.

Therefore, based on the above analysis, the RF path phase shifter architecture has the advantage of small area and easy system implementation. The RF phase shifter at 60 GHz requires low loss and large bandwidth. As only one mixer is needed for the entire array, the core circuitry of the receiver can be reused for multiple array configurations, without adding additional mixers to the circuitry, which makes it simple to extend to multiple antennas. Therefore, the main challenge is to design and implement a phase shifter with good phase accuracy, low loss, small phase variation, and small loss deviation.

2 60 GHz mm-Wave Phased Arrays Linkbudget

Based on the equation of free-space loss[1], the path is quadratic grow with the frequency. At 60 GHz, path loss is 82 dB for a 5 m wireless link. The signal is further attenuated by obstructions between the transmitter (TX) and RX, depending on the material. Brick wall attenuation is found to be 20 dB, concrete wall to be as high as 70 dB, while path loss due to person obstructing ranges from 10 dB to 20 dB[1]. With a typical RX performance, Fig.7 presents a 60 GHz communication link budget example for a 5 m distance and about 7 Gb/s data rate[8,12-16]. The desired SNR is 25 dB using 16-QAM modulation scheme with a bit-error-rate (BER) allowance of 10—12. The line-of-sight (LOS) signal is attenuated by 20 dB of people obstruction and the corresponding EIRP is 53 dBm. With the typical on-chip CMOS PA performance ranging from 10 dBm to 15 dBm[17-18], 20 dBi high-gain antennas are required both in TX and RX. However, such a high gain antenna has a very narrow beam width (approximate 17°), which is not robust if RX and TX are not fixed. Inversely, a low gain antenna with a higher PA output power makes it difficult to integrate the whole system on single chip.

With on-chip phase shifters, phased arrays can achieve a high antenna gain and directional beam steering capability. The propagation path loss is assumed to be 10 dB[1]. Fig.7 illustrates an example link budget for 60 GHz wireless link at 5 m using 16-

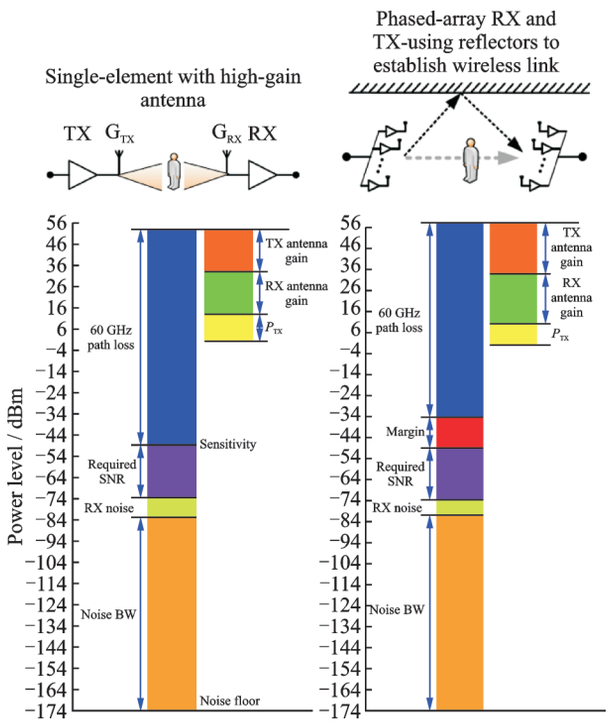

Fig.7 Single-element and phased array 60 GHz link budget

element phased array TX and RX structures. Assuming that the array gain provides 4 dB improvements compared with the single antenna gain, the TX power of each path is relaxed to 10 dBm. The reflected path loss at 5 m is 82 dB, plus the reflection loss of 10 dB. The SNR required for 16-QAM with 10^{-12} BER is 25 dB. In the end, the link is established with an additional margin of 15 dB, which means a higher order modulation scheme could be used for a higher date rate. Therefore, by using phased array setup, the link budget for 60 GHz wireless communication (8 Gb/s) is improved by 15 dB, accommodated with a relaxed requirement of PA output power and a reflected path as shown in Table 3.

Table 3 60 GHz link budget compared with phased arrays

Parameter	Single-element	Phased array
Channel bandwidth/MHz	2 160	2 160
TX power/ dBm	13	10
RX antenna gain/ dBi	20	24
TX antenna gain/ dBi	20	24
RX noise figure/ dB	7	7
Path loss @ 5m/ dB	82+20 (people obstruction 20 dB)	82+10 (10 dB reflection)
SNR requirement for 16-QAM / dB (BER 1e−12)	25	25
Noise bandwidth/ dB	93	82

Fig.8 shows a block diagram of a receiver front-end, which consists of a low-noise amplifier (LNA), a phase shifter, and a variable gain amplifier (VGA). The phase shifter has the function of changing the phase in the RF path. This could enable the electronics antenna beam scanning in the array architecture. The VGA has the function of providing adjustable gain for different phase. This could make the total RF gain flatter in the front-end. The LNA is located in front of the phase shifter and VGA to suppress the noise from later stages.

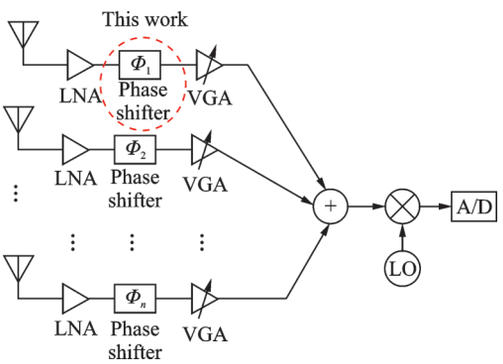

Fig.8 Block diagram of a receiver front-end for an RF phased-array system

3 mm-Wave Phase Shifter

In the analog domain, phase shifters could be implemented by using structures of switch-type[19-20], vector-sum[21-22] or reflection-type[23-24]. Vector-sum phase shifters provide the required phase delay by adjusting the weighting of the quadrature-phased signals. Reflection-type phase shifters are popular for continuous phase tuning, controlled by tunable varactor loads. However, phase shifters using these two techniques require a high-resolution DAC to provide the specific phase shift. Also the bad isolation between the RF and digital signals will degrade the DAC performance. Therefore, a switch-type digitally controlled phase shifter is better than the others. It is more robust than the others to the on-chip interference.

The switch-type phase shifters are typically implemented with 4 control bits[25-26] or 5 control bits[27-29] to satisfy the requirement of angle resolution and phase delay resolution. A 5 bit digitally controlled phase shifter has a phase delay resolution of 11.25° (a maximum phase error of ±5.625°). Fig.9 presents the array factor of a ULA 16-element phased array with 4 bit and 5 bit phase shifters, and an antenna spacing of $d=\lambda/2$. It can be seen that a 4 bit phase shifter is sufficient for all angles close to peak array gain.

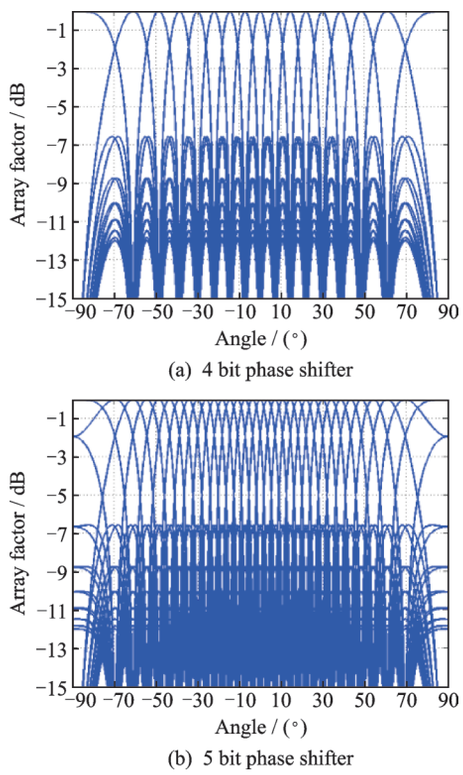

Fig.9 Array factor of a 16-element phased array with 4 bit and 5 bit phase shifter

Although a 4 bit phase shifter is sufficient for satellite communication and radar systems[27], it is not enough for high data rate (multi-Gbps) systems that uses high order modulation scheme such as 16-QAM or 64-QAM and large bandwidth. A 5 bit phase shifter has a smaller phase delay resolution to help reduce the error vector magnitude (EVM). It is also clear that the loss at the scanning direction due to the 4 bit phase resolution is less than 2 dB, while the loss could be suppressed to less than 0.5 dB if 5 bit phase shifter is used.

4 Phase Shifter Design Consideration

The phase shifter could be realized by high pass or low pass filter within 90°. Each of them

could be implemented in π or T structure (Fig.10). Because of the structure difference, the component value, L and C, will be different. Those differences will cause robust design issue, and we will discuss later. Beside the structure difference, the difference of the component value between the high pass filter and the low pass filter is also important, considering the robust issue. For phase delay less than 90°, the values of inductors and capacitors for the low or high-pass filter are calculated and summarized in Fig.10[28], where φ is the desired phase shift, Z_0 is the characteristic impedance, and ω_0 is the center frequency.

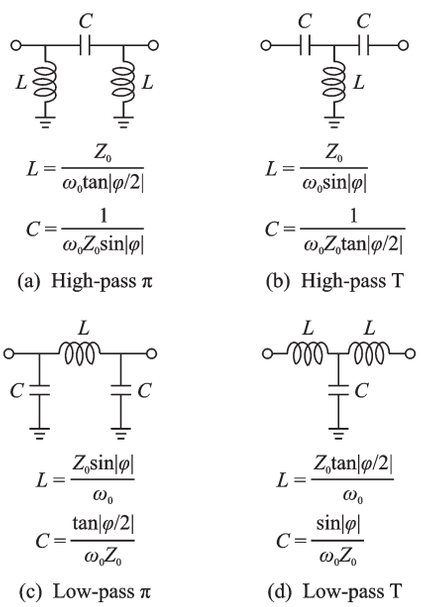

Fig.10 Different networks with insertion phase φ and matching to Z_0 at ω_0

The different component values are also plotted in Fig.11 as a comparison. In the low pass filter structure, the values of L and C are increasing with the frequency. While, it is decreasing with the frequency in the high pass filter. However, the L value is much larger in the high pass filter for small φ, which makes it difficult to implement on the CMOS technology with the reasonable performance. Considering the implementation issue and the parasitic, it is better to apply the low pass filter for the small φ instead of the high pass filter. On the other hand, the passive components are too small if using low pass filters. This would make the design more sensitivity to process variation. For example, to provide 11.25° phase shift, the required value for inductor and capacitor are 25.9 pH and 5.2 fF (low-π), 13 pH and 10 fF (low-T). Although low-π network has the advantage of only one inductor (area), the capacitor is too vulnerable to process variation. For low-T networks, as long as the two closely located inductors would not be too big to suffer from inductor coupling, T networks are better choice to implement of all the four networks.

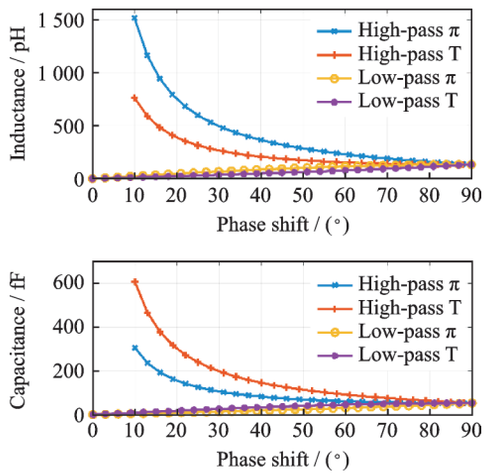

Fig.11 Different component values of four networks with insertion phase φ and matching to Z_0 at ω_0

The hybrid structure, shown in Fig.12, is composed of high pass and low pass filters. The total phase shifter is the difference between two paths. In the 180° situation, the phase achieved is the difference between 90° phase delay from the low pass filter and the 90° phase ahead by the high pass filter. In this way, it can take advantage of the different frequency property of high pass and low pass filters, and the whole frequency response is much flat and broadband. Also compared with the cascade of two identical high/low pass structures, hybrid structure provides the parallel connection. In this way, the loss is equal to original one stage instead of cascaded two stages. Therefore a hybrid structure avoids the cascading of phase deviation and passive losses.

Fig.13 illustrates the basic working mechanism of a single stage T-type phase shifter, which generates the phase delay by switching between the low-pass state when the phase shifter is on and the by-pass state when the phase shifter is off with zero

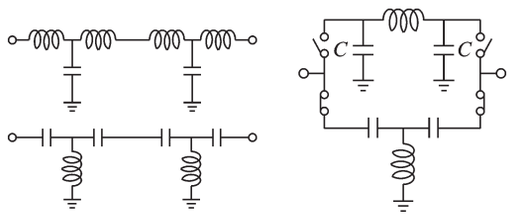

Fig.12 180° stage implementation

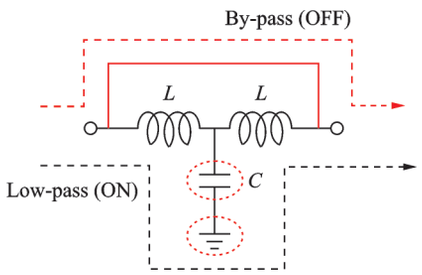

Fig.13 Working mechanism of a single stage T-type phase shifter

phase shifts. Therefore, a switch is needed to switch from different states. Besides, such structure suffers from ground problem that when the low-pass state is on, an ideal ground is needed to compose a low pass filter with accurate delay, while the by-pass state is on, an ideal open is needed to get rid of the low pass filter. Fortunately, a LC tank with capacitor implemented by transistor could solve this problem. Additionally, the capacitor that forms the low pass filter could also be implemented by transistors which suffer less from process variation.

Fig.14 shows the schematic of a single stage T-type switch-type phase shifter and its equivalent circuits for different states. When the low-pass state is on, transistors Q_1, Q_2 are turned off and Q_3 is turned on, the equivalent circuit forms a low pass filter and transistor Q_3 provides path to ground with a small on-resistance R_{on}. When by-pass state is on, transistors Q_1, Q_2 are turned on and Q_3 is turned off, and the equivalent circuit forms a by-pass state. The parasitic capacitance of transistor Q_3 and L_2 forms an LC resonator, providing an open port. Therefore, these two equivalent circuits will provide the desired phase shift at the frequency band.

The switches inside the phase shifter are implemented by N-metal oxide semiconductor (NMOS) transistors. A large biased resistor is added at the gate of this NMOS transistor to prevent signal leak-

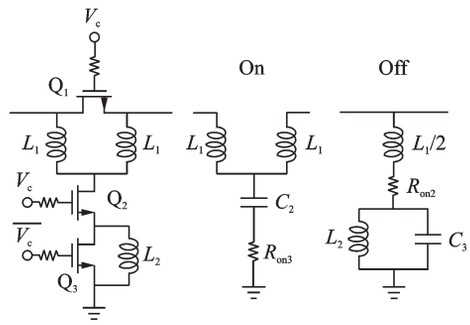

Fig.14 Schematic of a single stage T-type phase shifter

ing and oxide breakdown. The insertion loss of the transistor-based switch is affected by the source/drain junction capacitance, on-state resistance and the coupling with substrate. In the technology, the NMOS transistor can be fabricated in deep n-well structure. In the deep n-well technology, the extra n-well is implanted between the P-type silicon and the transistor. In this way, the body bias voltage can be connected to the source to reduce the insertion loss. Body-source connected and body-grounded transistor-based switches are analyzed and compared.

The equivalent circuit of CMOS transistor with deep-sub n-well technology is shown in Fig.15. The insertion loss arises from the coupling of drain (D) and source (S) nodes through junction capacitor C_{db} and C_{sb} to ground (G) at high frequencies and the on-resistor R_{ds} at low frequencies. When the source and body (B) are connected, the insertion loss decreases as the ground path through the substrate is removed. On the other hand, when the switch is turned off, the drain and source are connected directly through C_{db} since the source and body are connected together, which degrades the isolation of the switch. The on-state resistance could be reduced by increasing the size of transistors, which also introduces larger junction capacitor, resulting in more loss and poorer isolation.

Fig.16 illustrates the simulation results of insertion losses for body-grounded and body-source connected switches and it is clear that the insertion loss has a 0.5 dB improvement at 60 GHz when the body-source connected transistor is used. Simulation shows that there is an optimum value for the transis-

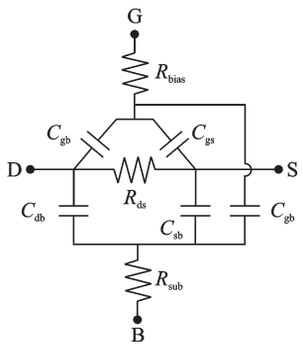

Fig.15 Equivalent-circuit diagram of NMOS transistor

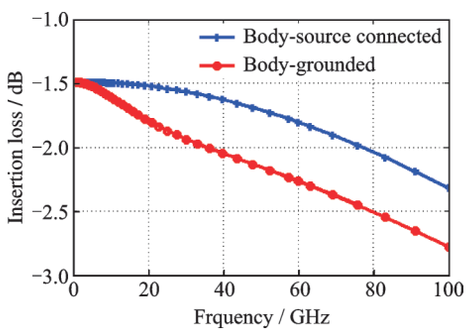

Fig.16 Simulated insertion loss of transistors with body connected to source and body-grounded

tor size to minimize the insertion loss while the isolation performance is decreasing as transistor becoming wider. Besides, the transistor switch with body-source connection could improve the insertion loss at the cost of isolation.

The phase shifter is implemented with five-degree stages with the fine resolution of 11.25°. The sequence of phase shifting stages is important for phase shifter with low phase variation and good inter-stage matching is affected by adjacent stages due to loading effects. Small phase shifting stages have smaller inductors and capacitors and thus are more sensitive to mismatches and loading effects than large phase shifting stages. Therefore small phase shifting stages, such as 11.25° stage and 22.5° stage are located in a position between large phase shifting stages to reduce influence of loading effect and have better phase linearity, as shown in Fig.17 .

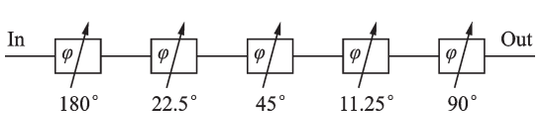

Fig.17 Sequence of degree stages of proposed 5 bit switch-type phase shifter

5 A 5 bit Passive Phase Shifter in 40 nm CMOS Technology

A 5 bit digitally controlled phase shifter is implemented by using five stages of switch-type delay networks. The 180° stage is composed by switching between low pass and high pass networks. Following 22.5°, 45°, and 11.25° stages are implemented by using low-pass T-type networks, and switching between low-pass state and by-pass state. The 90° stage is implemented by a π-type network. Because the inductor sizes are large and located nearby, they will suffer from coupling problem. For low insertion loss, the transistor switches are implemented with body-source connection. The schematic of the proposed 5 bit 60 GHz phase shifter is shown in Fig.18. The die photo of this phase shifter is shown in Fig. 19 with a core chip area of 600 μm × 400 μm (0.24 mm^2).

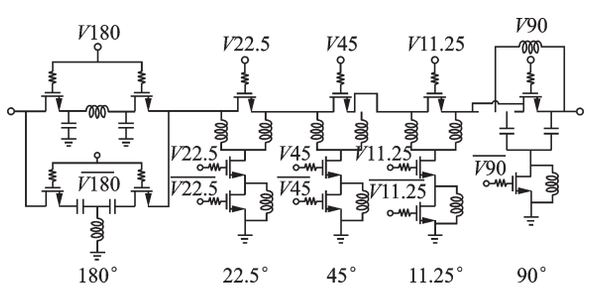

Fig.18 Simplified schematic of 5 bit switch-type phase shifter

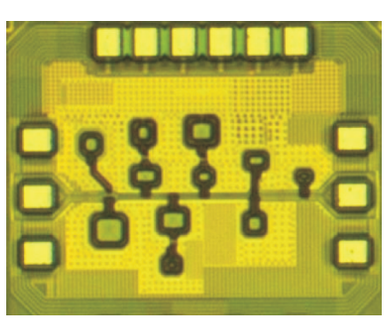

Fig.19 Die micro-graph of a 5 bit switch-type phase shifter in a 40 nm CMOS technology

The measured insertion phases of the 32 phase settings are depicted in Fig.20(a). The phase step is approximately 11.25°. Fig.20(b) highlights the relative phase shifts for 32 phase settings by setting the phase state 00000 as a reference. This shows that the 5 bit phase shifts are relatively constant over a

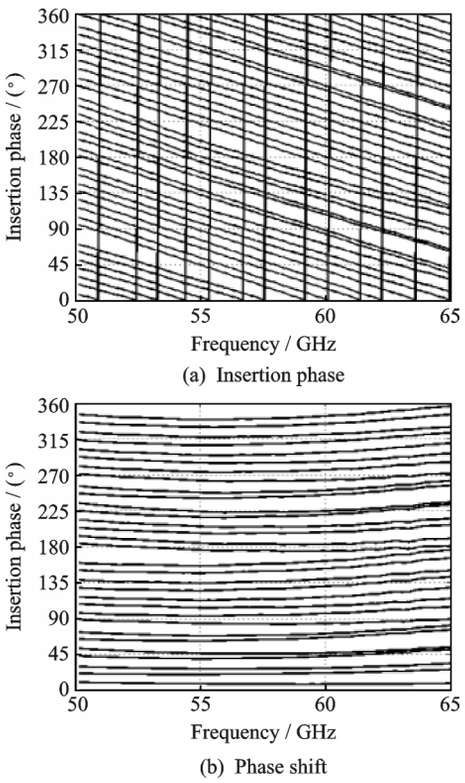

Fig.20 Measured insertion phase and relative phase shift of 32 different phase states from 50—65 GHz

wide frequency range. Derived from the measured insertion phase and gain shifts, Fig. 21 shows the measured RMS phase errors and RMS gain errors of the 32 phase states, giving 5° RMS phase error and 2 dB RMS gain errors at 60 GHz.

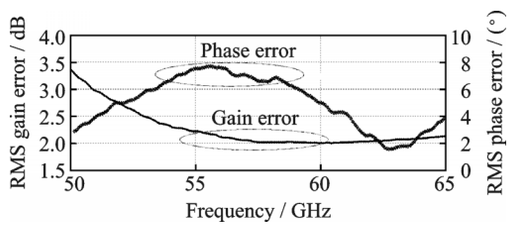

Fig.21 Measured RMS phase and gain errors of the phase shifter

Table 4 summarizes the measured circuit performance and compares to recently published RF phase shifters. The phase shifter has a lower phase deviation than other works, and at the same time keeps a comparable loss. Compared with the other RF phase shifters, the proposed 5 bit phase shifter has less phase error and less area, while achieving a comparable linearity and loss without ultra-thick metal.

Table 4 Performance summary and comparison

Reference	Ref.[25]	Ref.[26]	Ref.[30]	Ref.[31]	This work
Technology	0.18 μm SiGe	0.13 μm SiGe	65 nm CMOS	90 nm CMOS	40 nm CMOS
Frequence / GHz	40—45	57—64	55—65	57—64	57—65
Phase range / (°)	360	180	360	360	360
Resolution / (°)	n/a	n/a	22.50	11.26	11.25
Max loss / dB	12.5	8.0	16.0	18.0	20.9
Loss flatness / dB	n/a	±1.5	±2	±0.8	±1
Max phase error / (°)	9	n/a	9.2	10	6.8
Min phase error / (°)	6.5	n/a	5.5	2.0	1.5
Gain deviation / dB	n/a	n/a	n/a	1.8	2
P_{DC} / mW	40	0	0	0	0
Area / mm^2	0.11	0.56	0.2	0.34	0.24

6 Conclusions

In 5G and 6G wireless communication, 60 GHz frequency band is an essential part of the global spectrum. In 60 GHz mm-wave front-end, the phased array architecture can increase SNR. Therefore, it can enhance the wireless communication capacitor and enlarge the frequency coverage. In a phased array front-end, the phase shifter plays a core part for achieving the beam steering function. The phase shifting function could be implemented in the RF path, LO path and IF path. Compared with others, the RF path shifting could benefit the system by relaxing the linearity requirement,

which could save the system power consumption. In the phase shifter, there are active topology and passive topology. Compared with the active topology, the passive topology could save power consumption and provide a decent resolution. However, the value of passive component limits the passive phase shifter implementation. In this paper, a hybrid structure based 5 bit digitally controlled phase shifter is implemented in a 40 nm CMOS technology. By using this hybrid structure, the phase shifter could achieve balanced performance on phase accuracy, signal loss, and chip area. For all 32 states, the minimum phase error is 1.5°, and the maximum phase error is 6.8°. The measured insertion loss is -20.9 ± 1 dB including pad loss at 60 GHz and the return loss is >10 dB over 57—64 GHz. The total chip size is 0.24 mm^2 with 0 mW DC power consumption.

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