A Nonlinear Control Strategy for Vienna Rectifier Under Unbalanced Input Voltage

*REN Xiaoyong**, *CHEN Yu*, *TONG Dan*, *ZHANG Zhiliang*, *CHEN Qianhong*

Aero-Power Sci-Tech Center, College of Electronic Engineering, Nanjing University of Aeronautics and Astronautics, Nanjing 210016, P. R. China

(Received 15 May 2019; revised 10 July 2019; accepted 15 August 2019)

Abstract: The Vienna rectifier with unbalanced input voltage and load transient is analyzed. A nonlinear control strategy for Vienna rectifier under unbalanced input is proposed. From the view of positive and negative sequence components, the proposed nonlinear control strategy suppresses the twice frequency ripple and guarantees the dynamic response characteristic at the same time. Thanks to the proposed nonlinear control strategy, the DC bus capacitor can be reduced a lot since the voltage ripple and drop can be suppressed. A 10 kW Vienna rectifier is built to verify the proposed control strategy. After applying the proposed nonlinear control strategy, the voltage ripple is only 7 V and decreases over 75% over the traditional PI control when the unbalanced degree is 20%. The voltage drop can be reduced about 80% than former control strategy which is helpful to reduce the DC bus capacitor and achieve higher power density. The volume of the capacitor can be reduced by 83.3% with the new control method.

Key words: Vienna rectifier; radars; unbalanced input voltage; nonlinear control strategy; DC bus capacitance

CLC number: TM461 **Document code**: A **Article ID**: 1005-1120(2019)05-0703-12

0 Introduction

The increasing demand for high-power applications makes the application of three-phase PWM rectifiers more and more extensive. Among them, Vienna rectifier, as a three-level topology, has become the hotspot due to the advantages of low voltage stress, high power density, high efficiency and low total harmonic distortion (THD)[1]. Therefore, it is widely used in data center, telecom and aerospace power systems[2-4].

Since Vienna rectifier is a unidirectional converter, there could be twice power frequency ripple of the DC bus voltage when input voltage unbalance occurs in different phases[5]. In Vienna rectifier, the DC bus capacitor plays an important role since it can be increased purposely to suppress the twice frequency ripple. However, it should not be too large in order to achieve load transient performance[6-7]. However, too many capacitor will increase the volume therefore sacrifice the power density. A traditional control strategy is to make the input phase current track the input voltage. Nevertheless, it cannot eliminate the input power ripple and output dc-link voltage ripple[8-9]. In Ref.[10], a current loop based on proportional resonant (PR) controller has been achieved according to the model under unbalanced input. It can achieve good input and output characteristics under unbalanced input, but it hurts the dynamic performance. Refs.[11-12] used passive control and sliding mode control respectively to optimize the dynamic performance of the nonlinear system, however, and these two methods are all based on balanced input, which is not suitable for unbalanced input voltage. Same thing happens in the load feed forward digital control scheme to optimize dynamic performance[13]. Ref.[14] used a digitized feed forward compensation to optimize the dynamic

*Corresponding author, E-mail address: renxy@nuaa.edu.cn.

How to cite this article: REN Xiaoyong, CHEN Yu, TONG Dan, et al. A Nonlinear Control Strategy for Vienna Rectifier Under Unbalanced Input Voltage[J]. Transactions of Nanjing University of Aeronautics and Astronautics, 2019, 36(5): 703-714.

http://dx.doi.org/10.16356/j.1005-1120.2019.05.002

while this will improve the complexity of the control system and increase the requirement of the MCUs.

According to the model under the unbalanced input voltage, a nonlinear control strategy is proposed in this paper to obtain good performance for both steady and transient states. In the proposed nonlinear method, passive control for the current loop and sliding mode control for the voltage loop have been combined to guarantee a good dynamic response. With the new nonlinear control strategy, the DC bus capacitor can be reduced a lot since good steady state and dynamic performance can be obtained at the same time even under unbalanced input voltage.

This paper is organized as follows. In Section 1, based on the mathematical model for Vienna rectifier under unbalanced input, the problems under traditional PI controller have been analyzed. In Section 2, a novel nonlinear control strategy has been proposed to optimize the steady state characteristics under the unbalanced input voltage and dynamic response under the transient load. In Section 3, the experimental results are presented and discussed to verify the proposed nonlinear control strategy. Finally, the main points of this paper are summarized in Section 4.

1 Problems with Traditional Control Strategy for Vienna Rectifier

1.1 Operation property of Vienna rectifier

Fig.1 shows the structure of the Vienna rectifier. R_l and L_a, L_b, L_c are the equivalent resistance of input and boost inductors of each phase. S_a, S_b and S_c are the power switches of each phase. C_1, C_2 and R_o are the DC bus capacitors and the equivalent load of rectifier. u_a, u_b, u_c, i_a, i_b, i_c are three-phase instantaneous input voltages and currents. i_{pk}, i_{qk} and i_{nk} ($k=a, b, c$) are currents flowing through the upper diode, power switches and lower diode, respectively. U_{C1}, U_{C2} and U_{dc} are the rectified output voltages of upper capacitor, lower capacitor and total DC bus. i_p and i_n are the currents through the positive and negative dc-bus. i_M is the current flowing through the midpoint M.

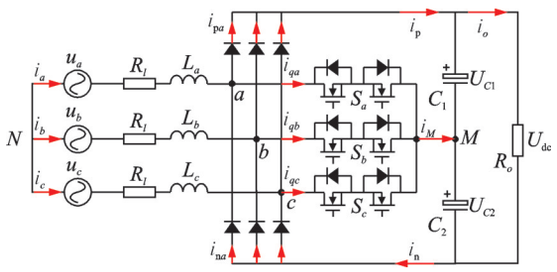


Fig.1 Topology of the Vienna rectifier

Under balanced condition, where $i_a+i_b+i_c=0$ and $u_a+u_b+u_c=0$. S_k ($k=a, b, c$) are the switching states of the bidirectional switch in Fig.1, then the switching functions can be defined as: $S_k=1$ means the switch is on; $S_k=0$ means the switch is off. If the neutral voltage is balanced ($U_{C1}=U_{C2}=U_{dc}/2$), u_i can be given as

$$u_i=\begin{cases}0 & S_i=1\\ \dfrac{U_{dc}}{2}\operatorname{sign}(i_i) & S_i=0\end{cases}\quad i=a,b,c \tag{1}$$

According to Kirchhoff's voltage law, the mathematical model of Vienna rectifier under dq rotating reference frame can be derived as

$$\begin{aligned}L\frac{\mathrm{d}i_d}{\mathrm{d}t}&=-R_l i_d+\omega L i_q-\frac{1}{2}U_{dc}S_d+u_d\\ L\frac{\mathrm{d}i_q}{\mathrm{d}t}&=-R_l i_q-\omega L i_d-\frac{1}{2}U_{dc}S_q+u_q\\ C\frac{\mathrm{d}U_{dc}}{\mathrm{d}t}&=\frac{3}{2}i_d S_d+\frac{3}{2}i_q S_q-\frac{2U_{dc}}{R_o}\end{aligned} \tag{2}$$

where u_{dq}, i_{dq}, S_{dq} represent the components of three-phase instantaneous input voltage, input current and switching states under dq rotating reference frame.

1.2 Problems with traditional control strategy under unbalanced voltage

Under balanced case, the typical control loop of the system under dq rotating reference frame is shown in Fig.2, where PI controller is adopted in both the voltage and the current loop.

The output of the voltage loop is applied as the current reference of d-axis i_d^*. The current reference of q-axis i_q^* is set zero. The output of the current loop is sent to the SVPWM module to generate the drive signal for each phase. The modulation strategy

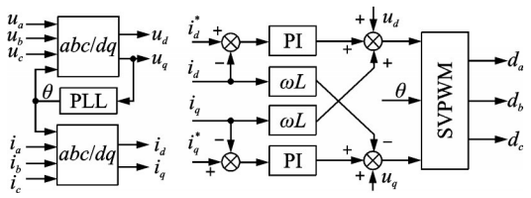


Fig.2 Traditional control strategy under dq rotating frame

applied here is the equivalent SVPWM[15-16]. ωL is added as a coefficient to realize the power decoupling between d-axis and q-axis.

There will be twice power frequency ripple of the output voltage when the rectifier works under unbalanced condition. In addition, the PI controllers used in control loop will inevitably cause ripple of the output voltage when three phase voltage are unbalanced or the load changes dynamically. Therefore, when the input or output conditions of the Vienna rectifier changes, its input and output characteristics will also be affected due to the poor anti-disturbance performance. In this case, in order to limit the output voltage ripple to a certain range, large capacitance is required and it will definitely influence the power density.

Fig. 3 shows d-axis current inner loop control block diagram of traditional double-loop control strategy of Vienna rectifier under dq rotating reference frame.

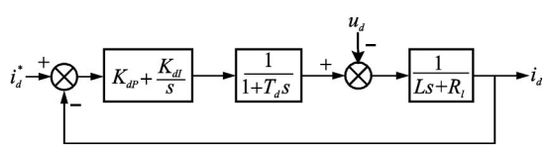


Fig.3 Control loop of the d-axis current

Corresponding transfer function of d-axis current inner loop can be achieved

$$G_{id}(s)=\frac{s(1+T_d s)(Ls+R_l)}{s(1+T_d s)(Ls+R_l)+(K_{dP}s+K_{dI})} \tag{3}$$

where $K_{dP}+K_{dI}/s$ is the transfer function of the PI controller, $1/(1+T_d s)$ the delay time of current sample and DSP controller, and $1/(Ls+R_l)$ the transfer function of the main circuit. According to Routh Criterion, the control system is stable since all the the closed-loop feature roots are on the left side of the imaginary axis.

However, for unbalanced three-phase input voltage, there would be twice power frequency component in the instantaneous active power and reactive power, which means the input current i_d and i_q have twice frequency disturbance

$$I^*_{d(2\omega)}(s)=\frac{K_1 s}{s^2+(2\omega)^2} \tag{4}$$

where K_1 is a constant. Then the response of current error to the disturbance can be obtained

$$E_{(i^*_d-i_d)}(s)=I^*_{d(2\omega)}(s)\cdot G_{id}(s)=\frac{K_1 s^2(1+T_d s)(Ls+R_l)}{[s^2+(2\omega)^2]\cdot[s(1+T_d s)(Ls+R_l)+(K_{dP}s+K_{dI})} \tag{5}$$

The denominator of Eq.(5) includes a pair of conjugate poles $s_{1,2}=\pm j2\omega$, which means this equation does not satisfy the final value theorem condition of Laplace transform[17]. In other words, the PI controller cannot realize tracking control without static error when variables contain twice frequency components.

Fig. 4 shows the steady state waveforms of a Vienna rectifier system with unbalanced input voltage.

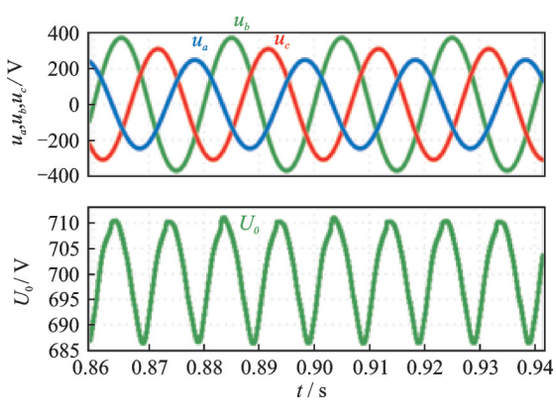


Fig.4 Steady state waveforms of input current and output voltage under unbalanced input

The parameters involved in the simulation system are listed in Table 1.

As shown in Fig.4, there is apparent distortion of the current waveform. Additionally, the waveform of the DC bus voltage has twice power frequency ripple $\Delta U_{bus}=25$ V which will influence the steady state performance of the system. In brief, the traditional model and control method cannot elimi-

Table 1 Parameters of simulation system

Parameter	Value
Input voltage $u_{a,\mathrm{rms}}$/V	220(−20%)
Input voltage $u_{b,\mathrm{rms}}$/ V	220(+20%)
Input voltage $u_{c,\mathrm{rms}}$/ V	220
Nominal power frequency f/Hz	50
Switching frequency f_s/kHz	34
Input inductor L/μH	350
Output voltage U_{dc}	700
Output capacitor C/μF	180(×6)
Output power P/kW	10

nate the twice power frequency component, thus the DC bus voltage ripple become obvious. Also, it will hurt the THD of input current and power factor (PF) eventually.

1.3 Problems with traditional control strategy under transient load

If the line impedance is ignored under the condition of unity PF, which means $i_q=0$ and $R_l=0$ in Eq.(2), then the d-axis current can be obtained

$$i_d=\left(\frac{Cu_{\mathrm{dc}}}{3}\frac{\mathrm{d}u_{\mathrm{dc}}}{\mathrm{d}t}+\frac{2}{3}u_{\mathrm{dc}}i_o\right)\Big/\left(u_d-L\frac{\mathrm{d}i_d}{\mathrm{d}t}\right) \quad (6)$$

where $i_o=U_{\mathrm{dc}}/R_o$ is the output current of the rectifier.

Discrete and formulate Eq.(6) when the rectifier works with pure resistive load

$$i_d(k+1)=\frac{Cu_{\mathrm{dc}}(k+1)\left[u_{\mathrm{dc}}(k+1)-u_{\mathrm{dc}}(k)\right]}{3t_s\left(u_d-L\dfrac{i_{\mathrm{dc}}(k+1)-i_{\mathrm{dc}}(k)}{t_s}\right)}+\frac{2u_{\mathrm{dc}}(k+1)i_o(k+1)}{3\left(u_d-L\dfrac{i_{\mathrm{dc}}(k+1)-i_{\mathrm{dc}}(k)}{t_s}\right)} \quad (7)$$

The reference of the d-axis current component is

$$i_d^*=(K_{\mathrm{dc}P}+K_{\mathrm{dc}I}/s)(u_{\mathrm{dc}}^*-u_{\mathrm{dc}}) \quad (8)$$

After performing discretization to Eq.(8), we can get

$$\begin{cases} i_d^*(k+1)=\left(K_{\mathrm{dc}P}+\dfrac{K_{\mathrm{dc}I}}{s}\right)\left[u_{\mathrm{dc}}^*(k+1)-u_{\mathrm{dc}}(k+1)+I_o(k)\right] \\ I_o(k)=K_{\mathrm{dc}I}t_s\sum_{m=1}^{k}\left[u_{\mathrm{dc}}^*(m)-u_{\mathrm{dc}}(m)\right] \end{cases} \quad (9)$$

When Vienna rectifier works at a steady state, such simplification can be achieved

$$\begin{cases} u_{\mathrm{dc}}^*(k+1)\approx u_{\mathrm{dc}}(k+1)\approx u_{\mathrm{dc}}(k+1) \\ i_d^*(k+1)\approx i_d(k+1)\approx i_d(k+1) \end{cases} \quad (10)$$

After combining Eqs. (7), (9), there is

$$\begin{cases} K_{\mathrm{dc}P}+\dfrac{K_{\mathrm{dc}I}}{s}=\dfrac{Cu_{\mathrm{dc}}(k+1)}{3t_s\left(u_d-L\dfrac{i_{\mathrm{dc}}(k+1)-i_{\mathrm{dc}}(k)}{t_s}\right)} \\ I_o(k)=\dfrac{2u_{\mathrm{dc}}(k+1)i_o(k+1)}{3\left(u_d-L\dfrac{i_{\mathrm{dc}}(k+1)-i_{\mathrm{dc}}(k)}{t_s}\right)} \end{cases} \quad (11)$$

where $[i_{\mathrm{dc}}(k+1)-i_{\mathrm{dc}}(k)]/t_s$ is the change rate of the d-axis current. Eq.(11) implies that the parameters of PI controller $K_{\mathrm{dc}P}$ and $K_{\mathrm{dc}I}$ in voltage loop are related to the output voltage and the change rate of the d-axis current. The parameters of main circuit such as L, C and the parameters of the controller such as $K_{\mathrm{dc}P}$ and $K_{\mathrm{dc}I}$ does not change when the rectifier is working. Accordingly, when the Vienna rectifier starts or has the transient load which means u_d changes, the output voltage u_{dc} will change too. Additionally, the PI controller has the lag part which will lead to a poor dynamic response when the load changes suddenly.

Fig.5 shows the waveforms of the output voltage when the load increases from 10% power to full power in Vienna rectifier whose parameters are listed in Table 1 under balanced condition. Since the control loop of output voltage uses traditional PI controller, the output voltage drops 55 V in Fig.5 which does not satisfy the limit of the voltage drop.

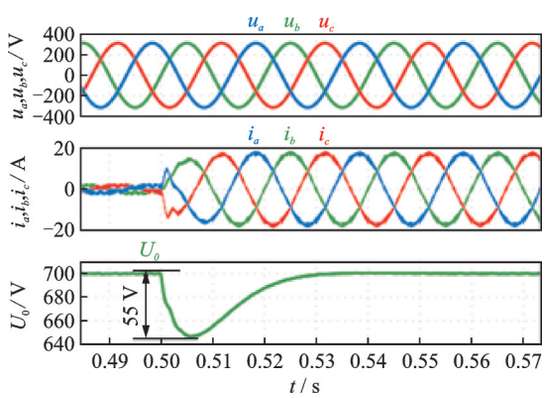


Fig.5 Dynamic waveforms of output voltage under load transient

From the analysis above, in order to solve the problems under unbalanced input and load tran-

sient, we need to optimize the mathematical model and control strategy and replace PI controller with nonlinear controller.

2 Proposed Nonlinear Control Strategy for Vienna Rectifier

2.1 Optimized mathematical model under unbalanced input voltage

Since the Vienna rectifier is a three-phase three-wire system, zero sequence component does not exist in the circuit. Therefore, the input voltage and current can be written into the sum of the positive and negative sequence component when three phase input is unbalanced

$$\begin{aligned} u_{abc}(t) &= u_{abc}^{+}(t) + u_{abc}^{-}(t) \\ i_{abc}(t) &= i_{abc}^{+}(t) + i_{abc}^{-}(t) \end{aligned} \tag{12}$$

Then the instantaneous active power $P_{\text{in}}(t)$ and reactive power $Q_{\text{in}}(t)$ can be achieved in Eqs.(13), (14). The instantaneous active power directly affects the output DC voltage.

$$\begin{aligned} P_{\text{in}}(t) &= u_{abc}\cdot i_{abc} = P_{\text{in\_0}} + \\ & P_{\text{in\_c2}}\cos(2\omega t) + P_{\text{in\_s2}}\sin(2\omega t) \end{aligned} \tag{13}$$

$$\begin{aligned} Q_{\text{in}}(t) &= u_{abc}^{\perp}\cdot i_{abc} = Q_{\text{in\_0}} + \\ & Q_{\text{in\_c2}}\cos(2\omega t) + Q_{\text{in\_s2}}\sin(2\omega t) \end{aligned} \tag{14}$$

$$\begin{cases} P_{\text{in\_0}} = u_d^{+}i_d^{+} + u_q^{+}i_q^{+} + u_d^{-}i_d^{-} + u_q^{-}i_q^{-} \\ Q_{\text{in\_0}} = u_d^{+}i_d^{+} - u_q^{+}i_q^{+} - u_q^{-}i_d^{-} + u_d^{-}i_q^{-} \\ P_{\text{in\_c2}} = u_d^{-}i_d^{+} + u_q^{-}i_q^{+} + u_d^{+}i_d^{-} + u_q^{+}i_q^{-} = Q_{\text{in\_s2}} \\ P_{\text{in\_s2}} = u_q^{-}i_d^{+} - u_d^{-}i_q^{+} - u_q^{+}i_d^{-} + u_d^{+}i_q^{-} = -Q_{\text{in\_c2}} \end{cases} \tag{15}$$

where $P_{\text{in\_0}}$ and $Q_{\text{in\_0}}$ are the DC components. The DC component of the reactive power $Q_{\text{in\_0}}$ determines the PF value when the circuit operates. $P_{\text{in}}(t)$ and $Q_{\text{in}}(t)$ also contain twice power frequency components including $P_{\text{in\_c2}}$, $P_{\text{in\_s2}}$, $Q_{\text{in\_c2}}$ and $Q_{\text{in\_s2}}$. The twice power frequency ripple will be introduced into the DC voltage, when $P_{\text{in\_c2}}$ and $P_{\text{in\_s2}}$ are not zero.

Eq.(15) gives the detailed expression of $P_{\text{in\_0}}$, $P_{\text{in\_c2}}$, $P_{\text{in\_s2}}$, $Q_{\text{in\_0}}$, $Q_{\text{in\_c2}}$ and $Q_{\text{in\_s2}}$. Since $P_{\text{in\_c2}}=Q_{\text{in\_s2}}$ and $P_{\text{in\_s2}}=-Q_{\text{in\_c2}}$, the ripple of the active power and inactive power can be eliminated at the same time. In order to realize the unity power factor and suppress the twice frequency ripple, the control targets can be set as: $Q_{\text{in\_0}}=0$, $P_{\text{in\_0}}=P_o$ and $P_{\text{in\_s2}}=P_{\text{in\_c2}}=0$. Therefore, current reference can be written as Eq.(16)

$$\begin{aligned} &\begin{bmatrix} i_d^{+*} & i_d^{-*} & i_q^{+*} & i_q^{-*} \end{bmatrix} = \frac{P_o^{*}}{K}\begin{bmatrix} u_d^{+*} & u_d^{-*} & u_q^{+*} & u_q^{-*} \end{bmatrix} \\ &K = \left[(u_d^{+})^2 + (u_q^{+})^2\right] - \left[(u_d^{-})^2 + (u_q^{-})^2\right] \end{aligned} \tag{16}$$

Compared with the current reference i_d^{*} acquired under the balanced input voltage in Section 1, the current reference i_d^{+*}, i_d^{-*}, i_q^{+*} and i_q^{-*} in Eq.(16) can guarantee none twice power frequency ripple at the DC bus even with unbalanced three-phase input. Combined with the traditional control loop in Fig.2, extra three PI controller are required in i_d^{-*}, i_q^{+*} and i_q^{-*} which will worsen the dynamic response a lot. Therefore, nonlinear control strategy is way more suitable here than the PI controller since it has better dynamic response than before.

2.2 Proposed current loop based on passive controller

Compared with PI controller, passive controller is a nonlinear control strategy from the view of energy, which can improve the dynamic characteristics. Therefore, passive controller is a better choice than PI controller for the current loop[18-19].

From the analysis in Section 2.1, the mathematical model of Vienna rectifier under unbalanced input can be written as Eq.(17).

$$\begin{bmatrix} L & & & & \\ & L & & & \\ & & L & & \\ & & & L & \\ & & & & C \end{bmatrix} \begin{bmatrix} \dfrac{\mathrm{d}i_d^{+}}{\mathrm{d}x} \\ \dfrac{\mathrm{d}i_q^{+}}{\mathrm{d}x} \\ \dfrac{\mathrm{d}i_d^{-}}{\mathrm{d}x} \\ \dfrac{\mathrm{d}i_q^{-}}{\mathrm{d}x} \\ \dfrac{\mathrm{d}u_{\text{dc}}}{\mathrm{d}x} \end{bmatrix} + \begin{bmatrix} 0 & -\omega L & & & \dfrac{S_d^{+}}{2} \\ \omega L & 0 & & & \dfrac{S_q^{+}}{2} \\ & & 0 & \omega L & \dfrac{S_d^{-}}{2} \\ & & -\omega L & 0 & \dfrac{S_q^{-}}{2} \\ -S_d^{+} & -S_q^{+} & -S_d^{-} & -S_q^{-} & 0 \end{bmatrix} \begin{bmatrix} i_d^{+} \\ i_q^{+} \\ i_d^{-} \\ i_q^{-} \\ u_{\text{dc}} \end{bmatrix} +$$

$$\begin{bmatrix} R_l & & & & \\ & R_l & & & \\ & & R_l & & \\ & & & R_l & \\ & & & & \frac{2}{R_o} \end{bmatrix} \begin{bmatrix} i_d^+ \\ i_q^+ \\ i_d^- \\ i_q^- \\ u_{dc} \end{bmatrix} = \begin{bmatrix} u_d^+ \\ u_q^+ \\ u_d^- \\ u_q^- \\ 0 \end{bmatrix} \tag{17}$$

According to the Euler-Lagrange (EL) equation, the above equation can be written into EL model

$$M\dot{x} + Jx + Rx = \varepsilon \tag{18}$$

where M is the energy storage term, J the connection term of internal interconnect structure, R the dissipative term and ε the input term of the system. From the point view of energy, the energy stored in C and L is always equal to the input energy of the system minus the energy dissipated in R_l and R_o.

Based on the passive controller theory, for a with multiple-input multiple-output (MIMO) system

$$\begin{cases} \dot{x} = f(\boldsymbol{x}, \boldsymbol{u}) \\ y = h(\boldsymbol{x}, \boldsymbol{u}) \end{cases} \tag{19}$$

where $\boldsymbol{x} \in \mathbf{R}^n$ is the state variable, $\boldsymbol{x} \in \mathbf{R}^m$ the input of the system, y the output of the system, f the partially continuous function on $(\boldsymbol{x}, \boldsymbol{u})$, and h the continuous function on $(\boldsymbol{x}, \boldsymbol{u})$. If there is a continuously differentiable semi-positive energy storage function $H(\boldsymbol{x})$ and a positive definite function $Q(\boldsymbol{x})$, for any $T>0$ the dissipative inequality satisfies Eq.(20), then the system is a strictly passive system.

$$H\left[x(T)\right] - H\left[x(0)\right] \leqslant \int_0^T \boldsymbol{u}^{\mathrm{T}} y \mathrm{d}t - \int_0^T Q(x) \mathrm{d}t \tag{20}$$

where $\boldsymbol{u}^{\mathrm{T}} y$ is the energy supply rate. Assuming that the total energy function of the Vienna rectifier is

$$H = \frac{1}{2} \boldsymbol{x}^{\mathrm{T}} M \boldsymbol{x} \tag{21}$$

From Eqs.(18), (21), there is

$$\dot{H} = \boldsymbol{x}^{\mathrm{T}} M \boldsymbol{x} = \boldsymbol{x}^{\mathrm{T}} (\varepsilon - Jx - Rx) \tag{22}$$

Since J_1+J_2 does not influence total energy of the system for it only reflects the structure, after integrating Eq.(22) on 0—T, we can get

$$H(T) - H(0) = \int_0^T \boldsymbol{x}^{\mathrm{T}} \varepsilon \mathrm{d}t - \int_0^T \boldsymbol{x}^{\mathrm{T}} R \boldsymbol{x} \mathrm{d}t \tag{23}$$

Therefore, the Vienna rectifier is a strictly passive system where passive control theory can be applied.

After substituting the error function $x_e = x - x^*$ into Eq.(18), the dynamic characteristic of the error system can be obtained

$$M\dot{x}_e + Jx_e + Rx_e = \varepsilon - (M\dot{x}^* + Jx^* + Rx^*) \tag{24}$$

According to the passive control theory, in order to make the error system dynamic characteristic converge to zero quickly, a dissipation term R_a need to be injected. The dissipation term after injection is $R_d = R + R_a$. Then, the new error system dynamic characteristic after injection can be obtained

$$\begin{aligned} &M\dot{x}_e + Jx_e + R_d x_e = \\ &\varepsilon - (M\dot{x}^* + Jx^* + Rx^* - R_a x_e) \end{aligned} \tag{25}$$

where R_a is the injected dissipation term and R the initial damp term. The control law can be achieved in Eq.(26) since $M\dot{x}_e + Jx_e + R_d x_e = 0$ need to be realized

$$\varepsilon = M\dot{x}^* + Jx^* + Rx^* - R_a x_e \tag{26}$$

After substituting Eq.(26) into Eq.(17), the switch function under passive controller can be achieved

$$\begin{cases} S_d^+ = 2\left[u_d^+ + \omega L i_q^+ - R_l i_d^{+*} + r_{a1}(i_d^+ - i_d^{+*}) \right]/U_{dc} \\ S_q^+ = 2\left[u_q^+ - \omega L i_d^+ - R_l i_q^{+*} + r_{a2}(i_q^+ - i_q^{+*}) \right]/U_{dc} \\ S_d^- = 2\left[u_d^- - \omega L i_q^- - R_l i_d^{+*} + r_{a3}(i_d^- - i_d^{-*}) \right]/U_{dc} \\ S_q^- = 2\left[u_q^- + \omega L i_d^- - R_l i_q^{-*} + r_{a4}(i_q^- - i_q^{-*}) \right]/U_{dc} \end{cases} \tag{27}$$

where i_d^{+*}, i_d^{-*}, i_d^{+*} and i_d^{-*} can be achieved by the outer voltage loop. After sending the switching function into the SVPWM module, the duty of each switch can be achieved to realize the control for the Vienna rectifier.

2.3 Proposed voltage loop based on sliding mode control

Compared with PI controller, sliding mode controller is a more suitable solution under unbalanced voltage input since the outer disturbance and change of the variables will not influence the operation of the system when it works on the sliding mode surface[20-21].

According to sliding mode variable structure control theory, the sliding mode surface is

$$\begin{aligned} &S(x_{e5}) = x_{e5} + m\frac{\mathrm{d}x_{e5}}{\mathrm{d}t} = \\ &x_5 - x_5^* + m\left(\frac{\mathrm{d}x_5 - \mathrm{d}x_5^*}{\mathrm{d}t}\right) = 0 \end{aligned} \tag{28}$$

where m ($m>0$) is the sliding mode coefficient, x_{e5} the input variable, x_5 the real value and x_5^* the reference. The larger m is, the less time the system takes to reach sliding mode. However, larger m will lead to a narrower area where the sliding mode exists. In the voltage control loop, the error between the DC bus voltage and the reference voltage $x_{e5}=x_5-x_5^*=u_{dc}-u_{dc}^*$ is chosen as the input variable.

According to Eq. (17), when the rectifier works under unbalanced input voltage there is

$$\frac{\mathrm{d}u_{dc}}{\mathrm{d}t}=\frac{S_d^+ i_d^+ + S_d^- i_q^+ + S_q^+ i_d^- + S_q^- i_q^- - 2i_o}{C} \tag{29}$$

Since the value of DC bus reference voltage will not change, $\mathrm{d}u_{dc}^*/\mathrm{d}t=0$. Then Eq. (28) can be written as

$$s(x_{e5})=u_{dc}-u_{dc}^*+m\left(\frac{S_d^+ i_d^+ + S_q^+ i_q^+ + S_d^- i_d^- + S_q^- i_q^- - 2i_o}{C}\right) \tag{30}$$

After substituting Eq.(16) into Eq.(30), there is

$$P_o^*=\frac{K\left[2i_o+\frac{C}{m}(u_{dc}-u_{dc}^*)\right]}{S_d^+ i_d^+ + S_d^- i_q^+ + S_q^+ i_d^- + S_q^- i_q^-} \tag{31}$$

When the system operates at a steady state, the reference value such as u_{dc}^* can be considered equal with u_{dc}. Then Eq. (16) can be written as

$$[\,i_d^{+*}\quad i_d^{-*}\quad i_q^{+*}\quad i_q^{-*}\,]=[\,i_d^+\quad i_d^-\quad i_q^+\quad i_q^-\,]=\frac{P_o}{K}[\,u_q^+\quad u_d^-\quad u_q^+\quad u_q^-\,] \tag{32}$$

Therefore, the switch function Eq.(27) can be changed to

$$\begin{cases} S_d^+ = 2(u_d^+ + \omega L i_q^+ - R_l i_d^{+*})/U_{dc} \\ S_q^+ = 2(u_q^+ - \omega L i_d^+ - R_l i_q^{+*})/U_{dc} \\ S_d^- = 2(u_d^- - \omega L i_q^- - R_l i_d^{+*})/U_{dc} \\ S_q^- = 2(u_q^- + \omega L i_d^- - R_l i_q^{-*})/U_{dc} \end{cases} \tag{33}$$

After substituting Eq.(33) into Eq.(29), the power reference under unbalanced input can be achieved

$$P_o^*=\frac{Ku_{dc}\left[2i_o+\frac{C}{m}(u_{dc}^*-u_{dc})\right]}{2\left(K-\frac{K_1}{K}R_l P_o\right)} \tag{34}$$

where the detailed expressions of K and K_1 are

$$\begin{cases} K=\left[(u_d^+)^2+(u_q^+)^2\right]-\left[(u_d^-)^2+(u_q^-)^2\right] \\ K_1=\left[(u_d^+)^2+(u_q^+)^2\right]+\left[(u_d^-)^2+(u_q^-)^2\right] \end{cases} \tag{35}$$

In order to optimize the design of controller, assuming $R_l=0$, then Eq.(34) can be simplified as

$$P_o^*=P_o+\frac{u_{dc}\cdot C}{2m}(u_{dc}^*-u_{dc}) \tag{36}$$

Fig. 6 shows the control loop of the sliding mode controller. As can be seen in Fig.6, the variable P_o^* is applied as the output of the voltage loop which is sent to the current loop to acquire the reference of the current based on Eq.(16).

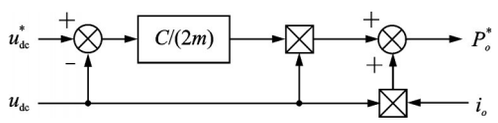


Fig.6 Control loop of the voltage loop

Fig. 7 shows the control block diagram of the proposed nonlinear control strategy. As can be seen in Fig. 7, the output of the rectifier i_o and U_{dc} are sent to the voltage loop where sliding mode control is applied. Then, the output of the voltage loop P_o^* is sent to the current reference diagram to get i_d^{+*}, i_d^{-*}, i_q^{+*} and i_q^{-*}. Finally, the current reference is sent to the current loop to get the duty of each phase.

The simulation has been built on the PLECS to compare two different control strategies under unbalanced input voltage. The parameters are the same with those in Table 1. When the load changes from to 10% load to full load, the waveforms are shown in Fig.8.

As can be seen in Fig.8 (a), the voltage drop under traditional control strategy is 40 V and the time it takes to achieve steady state is around 30 ms. Additionally, the twice frequency voltage ripple is 10 V. However, with proposed nonlinear control strategy, the voltage drop and the steady time are only 5 V and 8 ms, respectively, in which the twice frequency voltage ripple is only 0.5 V. The simulation results show that the proposed nonlinear control strategy has a better performance for both dynamic and steady states than the initial one.

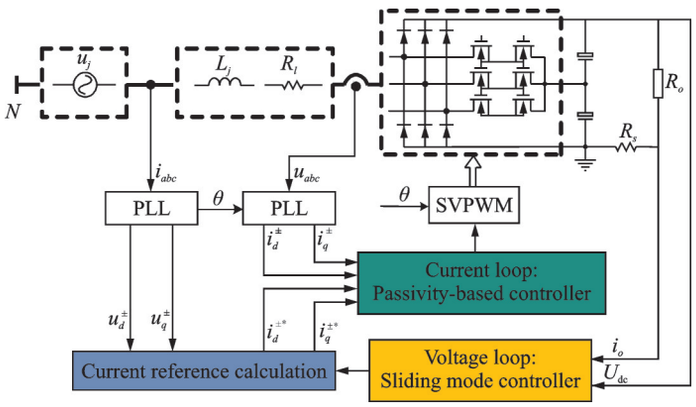


Fig.7 Block diagram of the proposed nonlinear control strategy

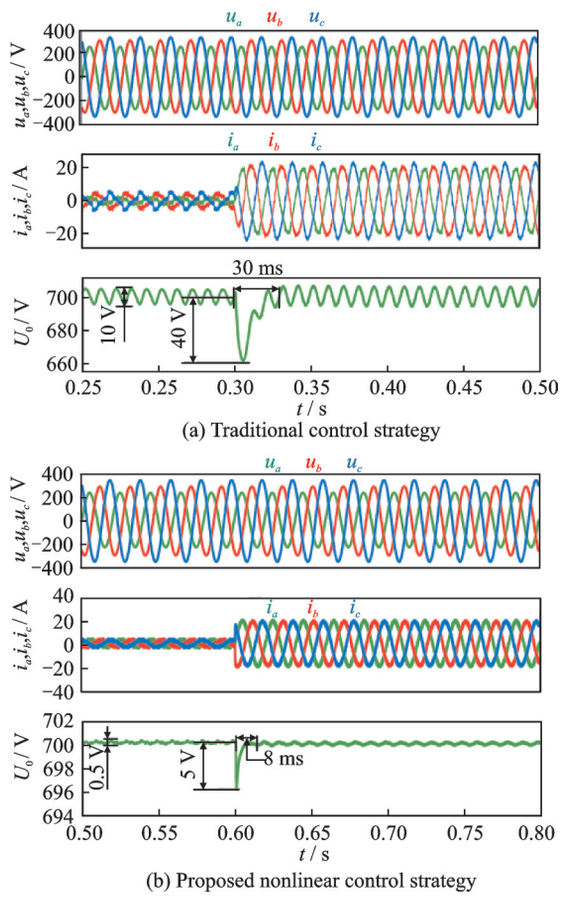


Fig.8 Simulation waveforms of DC link voltage under transient load

3 Experimental Verification

To verify the proposed nonlinear control strategy in Vienna rectifier under unbalanced input voltage, a prototype of 10 kW is built in Fig.9. The input phase-voltage of the convert is 220 V when three-phase voltage is balanced. The traditional control strategy is depicted in Fig.2, and the proposed nonlinear control is depicted in Fig.7. The constructed experiment is designed with the same parameters as those listed in Table 1. The controller of the prototype is implemented with TMS320F28075 DSP processor. The C28x floating point unit (FPU) fastRTS Library is applied here since it can realize the functions such as sinusoid and square root here. According to the application note of this library, the routines in this library can guarantee that the user can achieve execution speeds considerably faster than the past.

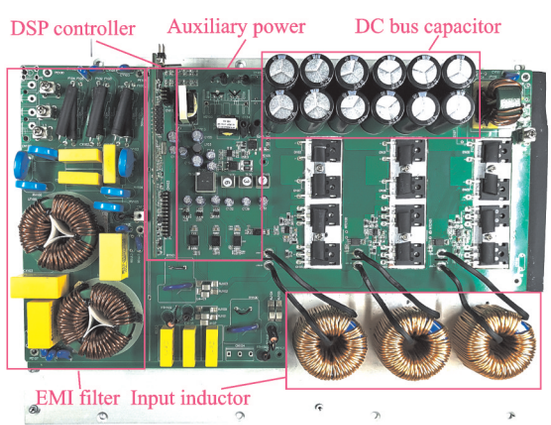
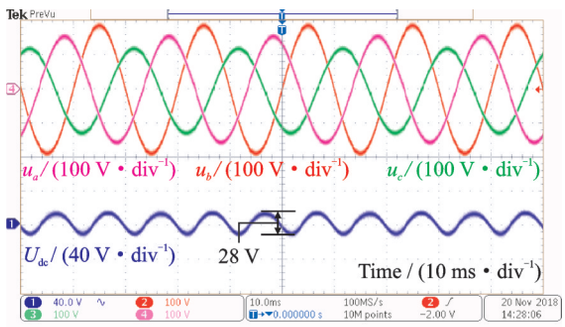


Fig.9 Experimental prototype

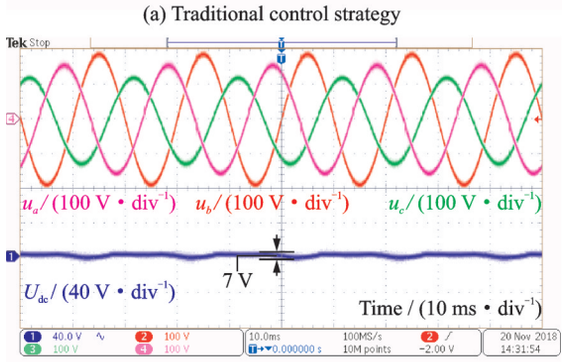
3.1 Steady state waveforms under unbalanced voltage

Fig.10 compares the waveforms of DC bus voltage when three-phase input is unbalanced. The voltage of phase A is 110 V, the voltage of phase B is 110 V(+20%) and the voltage of phase C is 110 V (−20%). The blue waveform is the DC bus voltage. From Fig.10(a), the amplitude of twice power frequency voltage reaches 28 V under traditional

control strategy. When the nonlinear control strategy is applied, the ripple can be reduced to 7 V that is only a quarter than the initial ripple. Accordingly, the voltage ripple can be reduced a lot under the proposed strategy.



(a) Traditional control strategy



(b) Proposed nonlinear control strategy

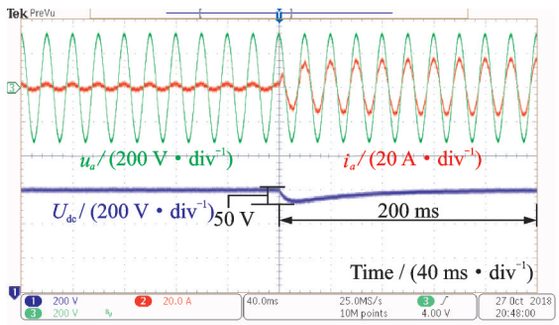
Fig.10 Waveforms of DC link voltage under unbalanced input

3.2 Dynamic waveforms under load transient

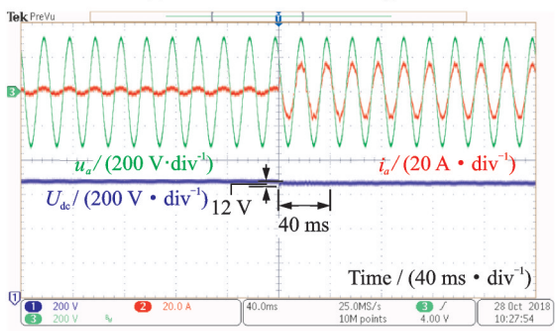
Fig. 11 compares the waveforms of the input voltage, input current and DC bus voltage when the power jumps from 1 kW to 8 kW. As can be seen in Fig. 11(a), the drop of the DC bus voltage can reach 50 V under the traditional control strategy. Besides that, the time it takes to return the steady state is 200 ms. However, the voltage drop is only 12 V when nonlinear control strategy is implemented and the time can be reduced to 40 ms. The quality of the current waveform will not be influenced a lot under the proposed control strategy. Hence the new control strategy can increase dynamic characteristic and decrease the voltage drop strikingly.

3.3 Capacitance decrease experiment

Since the proposed nonlinear control strategy can reduce the voltage drop when the load transient



(a) Traditional control strategy



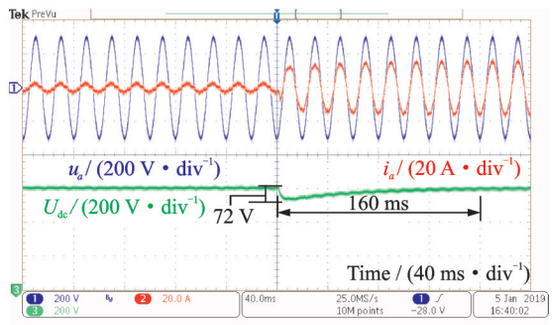
(b) Proposed nonlinear control strategy

Fig.11 Experimental waveforms of DC link voltage under transient load

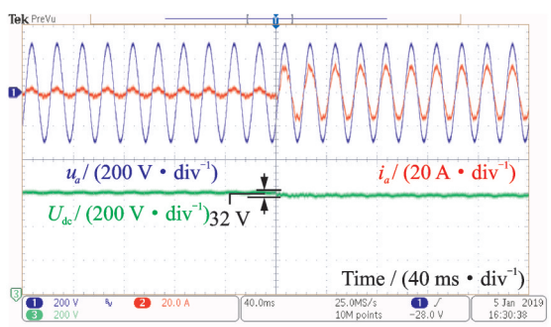
happens, the DC bus capacitor can be reduced to improve the power density of the rectifier. As can be seen in Fig.9, the initial capacitor of the prototype is 180 μF(×6). The waveforms of the DC bus voltage after reducing the capacitor to 180 μF(×3) are shown in Fig.12. As shown in Fig.12(a), the voltage drop under traditional control strategy can be 72 V that is unacceptable in the real operating condition. After applying the nonlinear control strategy, the voltage drop can be reduced to only 32 V less than the drop in Fig.12(a) when the capacitor is 180 μF(×6). Accordingly, the capacitor can be reduced with purpose when the new control strategy is implemented for this can guarantee the same or even better dynamic characteristic than the initial control.

3.4 The optimization of capacitance experiment

In order to achieve better performance of the steady state, the film capacitor and electrolytic capacitor are selected to absorb high frequency and low frequency current ripple, respectively. According to the rules of impedance matching[22], there is



(a) Traditional control strategy with 180 μF(×6)



(b) Proposed nonlinear control strategy with 180 μF(×3)

Fig.12 Waveforms of DC link voltage under transient load after reducing capacitor

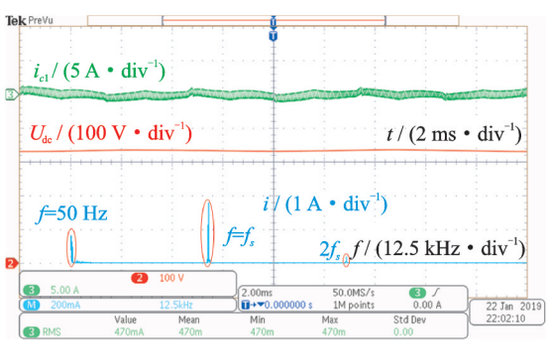
$$\begin{cases} X_1 = \dfrac{1}{2\pi f_s C_1} + 2\pi f_s L_1 \\ X_2 = \dfrac{1}{2\pi f_s C_2} \\ X_1 = 5X_2 \end{cases}$$

where C_1 is the electrolytic capacitor, and L_1 the inductor in series with C_1 and C_2 is the film capacitor. Since the value C_1 is much larger than C_1, the inductor L_1 is required to realize that the low-frequency current ripple mainly flow through the electrolytic capacitor. The ratio between low-frequency and high-frequency is selected as 5∶1 here. The detailed parameters of the capacitor are shown in Table 2.

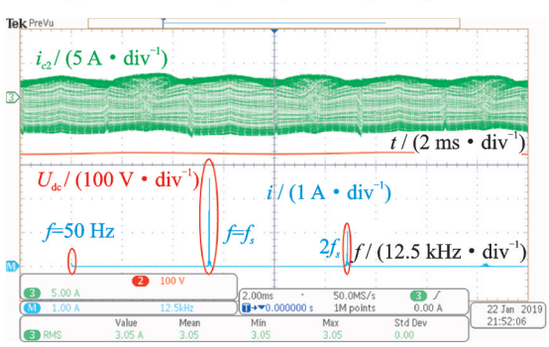
Table 2 Capacitor parameters

Supplier	Type	Value	Number
AiSHi	ELC2WM181O40KT	180 μF/450 V	3
KEMET	C4AEGBU5100A1XK	10 μF/450 V	1

Fig.13 shows the waveforms of current flowing through the electrolytic capacitor i_{c1} and the film capacitor i_{c2} when the output power is 4 kW. After performing Fourier decomposition, we can get the spectrum of current flowing through capacitors. By comparing Fig. 13 (a) and (b), we can find the low-frequency component of i_{c1} is much larger than i_{c2} which means the low-frequency ripple flows mainly through the electrolytic capacitor. On the contrary, the high-frequency current flows mainly through film capacitor since the high-frequency component of i_{c2} is far more than i_{c1}. It can also be found that current ripple at switching frequency of i_{c2} is nearly five times that of i_{c1}, which corresponds with the theoretical analysis. Therefore, the proposed CL-C connecting method can reduce the DC bus capacitance effectively and promise the same working performance.



(a) Current flowing through electrolytic capacitor



(b) Current flowing through film capacitor

Fig.13 Waveforms of DC link voltage and current under Fourier transform after reducing capacitor

3.5 Comparison of steady state efficiency

The efficiency of the convert under two control strategies is shown in Fig.14.

As shown in Fig.14, the comparison of efficiency indicates that the nonlinear control strategy will influence the efficiency a little which is 98% when the load is 8 kW. Although the total efficiency decreases 0.5%, the Vienna rectifier can still have a high power frequency.

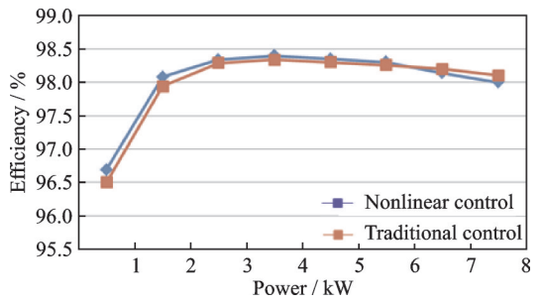


Fig.14 Efficiency of two control strategies under different load

4 Conclusions

A nonlinear control strategy in proposed in this paper to optimize the steady state performance and dynamic performance of the Vienna rectifier with unbalanced input voltage and load transient. From the view of positive and negative sequence component, the proposed nonlinear control strategy generated to suppress the twice frequency ripple caused by unbalanced input voltage. The current loop is based on the passive controller and the voltage loop is based on the sliding mode control which can guarantee the dynamic performance under load transient.

After applying the proposed nonlinear control strategy, the voltage ripple is only 7 V and decreases over 75% over the traditional PI control when the unbalance degree is 20%. The voltage drop can be reduced about 80% than former control strategy which is helpful to reduce the DC bus capacitor and achieve higher power density. Besides that, current ripple can be distributed effectively after applying the optimized CL-C connecting method as designed. The volume of the capacitor can be reduced by 50% with the new control method.

References

[1] KOLAR J W, ERTL H, ZACH F C. Design and experimental investigation of a three-phase high power density high efficiency unity power factor PWM (VIENNA) rectifier employing a novel integrated power semiconductor module[C]//APEC. [S. l.]: IEEE, 1996.

[2] KOLAR J W, FRIEDLI T. The essence of three-phase pfc rectifier systems—Part I [J]. IEEE Transactions on Power Electronics, 2013, 28(1): 176-198.

[3] HARTMANN M, ROUND S D, ERTL H, et al. Digital current controller for a 1 MHz, 10 kW three-phase vienna rectifier[J]. IEEE Transactions on Power Electronics, 2009, 24(11): 2496-2508.

[4] LIU B, REN R, JONES E, et al. A modulation compensation scheme to reduce input current distortion in GaN based high switching frequency three-phase three-level vienna type rectifiers[J]. IEEE Transactions on Power Electronics, 2017, 33(1): 283-298.

[5] MINIBOCK J, STOGERER F, KOLAR J W. A novel concept for mains voltage proportional input current shaping of a VIENNA rectifier eliminating controller multipliers. I. Basic theoretical considerations and experimental verification[C]//IEEE Applied Power Electronics Conference & Exposition. [S.l.]: IEEE, 2001.

[6] KANG S W, KIM S I, KIM R Y, et al. High power factor control of an inverter-controlled synchronous motor drive system with small DC-link capacitor[C]// Conference of the IEEE Industrial Electronics Society. [S.l.]: IEEE, 2014.

[7] TONG D, REN X, CHEN Y, et al. A nonlinear control strategy to reduce DC bus capacitance in Vienna rectifier[C]//2019 IEEE Applied Power Electronics Conference and Exposition (APEC). [S.l.]: IEEE, 2019.

[8] MINIBOCK J, KOLAR J W. Novel concept for mains voltage proportional input current shaping of a VIENNA rectifier eliminating controller multipliers[J]. IEEE Transactions on Industrial Electronics, 2005, 52(1): 162-170.

[9] RIOUAL P, POULIQUEN H, LOUIS J P. Regulation of a PWM rectifier in the unbalanced network state using a generalized model[J]. Power Electronics IEEE Transactions on, 1996, 11(3): 495-502.

[10] HANG L, ZHANG H, LIU S, et al. A novel control strategy based on natural frame for Vienna-type rectifier under light unbalanced-grid conditions[J]. IEEE Transactions on Industrial Electronics, 2015, 62(3): 1353-1362.

[11] CHEN B, MA H, XIE Y, et al. Sliding mode and predictive current control for Vienna-type rectifiers[C]//International Conference on Electrical Machines & Systems. [S.l.]: IEEE, 2015.

[12] SAHARI A A, MOUSAVIAN H, ZOLGHADRI M R, et al. A passivity-based controller via parallel damping injection for three phase/level/switch unity power factor (Vienna I) rectifier[C]//2008 11th Workshop on Control & Modeling for Power Electronics. [S.l.]: IEEE, 2008.

[13] CHEN X, REN X, ZHANG Z, et al. Dynamic response optimization for three-phase vienna rectifier with load feedforward control[C]//2016 IEEE Energy Conversion Congress and Exposition (ECCE). [S.l.]: IEEE, 2016.

[14] WANG L, ZHANG D, WANG Y, et al. Dynamic

performance optimization for high-power density three-phase Vienna PFC rectifier[C]//2015 IEEE 2nd International Future Energy Electronics Conference. [S.l.]: IEEE, 2015.

[15] BURGOS R, LAI R, PEI Y, et al. Space vector modulator for Vienna-type rectifiers based on the equivalence between two- and three-level converters: A carrier-based implementation[J]. IEEE Transactions on Power Electronics, 2008, 23(4): 1888-1898.

[16] HANG L, LI B, ZHANG M, et al. Equivalence of SVM and carrier-based PWM in three-phase/wire/level Vienna rectifier and capability of unbalanced-load control[J]. IEEE Transactions on Industrial Electronics, 2014, 61(1): 20-28.

[17] CORINTHIOS M J. A generalized transform, grouping, Fourier, Laplace and Z transforms[C]//The 14th International Conference on Microelectronics. [S.l.]:IEEE, 2002.

[18] DEL PUERTO-FLORES D, SCHERPEN J M A, LISERRE M, et al. Passivity-based control by series/parallel damping of single-phase PWM voltage source converter[J]. IEEE Transactions on Control Systems Technology, 2014, 22(4): 1310-1322.

[19] ZHANG Z, KANG L, XU H. A passivity-based controller for a unity-power-factor rectifier[C]//International Conference on Electrical Machines & Systems. [S.l.]: IEEE, 2013.

[20] YACOUBI L, AL-HADDAD K, DESSAINT L A, et al. Linear and nonlinear control techniques for a three-phase three-level NPC boost rectifier[J]. IEEE Transactions on Industrial Electronics, 2006, 53(6): 1908-1918.

[21] WU Y, FANG Y, LE L, et al. Global dynamic sliding mode control of PMSM speed servo systems base on extended state observer[C]//Proceedings of the 32nd Chinese Control Conference. [S.l.]: IEEE, 2013.

[22] ROY S C D. Characteristics of single- and multiple-frequency impedance matching networks[J]. IEEE Transactions on Circuits & Systems II Express Briefs, 2015, 62(3): 222-225.

Acknowledgements This work was supported in part by the National Natural Science Foundation of China (Nos. 51777093 ,51722702).

Authors Prof. **REN Xiaoyong** received the B.S., M.S. and Ph.D. degrees in Electrical Engineering from Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, P. R. China, in 2002, 2005 and 2008, respectively. From 2009 to 2011, he was a Postdoctoral Researcher at the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA. He is currently with the Department of Electrical Engineering, NUAA. His current research interests include DC-DC conversion, converter control techniques, GaN device application and renewable power systems.

Mr. **CHEN Yu** is currently working toward the M.S. degree at the Aero-Power Sci-Tech Center, NUAA. His research interests include high frequency GaN applications and the applications of three-phase Vienna rectifier.

Ms. **TONG Dan** received the M.S. degree in Electrical Engineering from NUAA, Nanjing, China, in 2016. Her research interests include high frequency GaN applications and digital control techniques for power electronic circuits.

Prof. **ZHANG Zhiliang** received the B.S. and M.S. degrees from Nanjing University of Aeronautics and Astronautics (NUAA), P. R. China, in 2002 and 2005, and Ph.D. degree from Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada, in 2009. From June to September 2007, he was a Design Engineering Intern from with Burlington Design Center, Linear Technology Corporation. He is currently a Professor with the Aero-Power Sci-Tech Center, NUAA. His research interests include high-frequency power conversion with wide bandgap devices.

Prof. **CHEN Qianhong** received the B.S. and Ph.D. degrees in electrical engineering from Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 1995 and 2001, respectively. She is currently a Professor with the Aero-Power Sci-Tech Center. From April 2007 to January 2008, she was a Research Associate in the Department of Electronic and Information Engineering, Hong Kong Polytechnic University, Hong Kong, China. Her research interests include application of integrated-magnetics, wireless power transfer. Dr. Chen is the director of the NUAA-ZTE Joint Laboratory of the communication wireless power transmission technology and one of the main sponsors of the high-power wireless transmission industry alliance in China.

Author contributions Prof. **REN Xiaoyong** contributed to guide of the total study. Mr. **CHEN Yu** contributed to design hardware platform, conduct the analysis and write the manuscript. Ms. **TONG Dan** contributed to write the program of DSP and comply the model. Prof. **ZHANG Zhiliang** contributed to guide of the circuit design. Prof. **CHEN Qianhong** contributed to guide of the magnets design. All authors commented on the manuscript and approved the submission.

Competing interests The authors declare no competing interests.

(Production Editor: Sun Jing)