Interleaved-Connected Split Planar Resonant Inductor Design in 1 kV SiC LLC Converters

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Abstract: Design method of split planar resonant inductor in 1 kV SiC logical link control (LLC) converter is proposed, which ensures the converter power density of 93.59 W/ in^3 and peak efficiency of 95.73%. Split resonant inductor helps to provide symmetrical resonant current by symmetrical impedance, and improves the distortion of resonant current, which ensures the efficiency of the whole converter. An interleaved winding connecting scheme improves the power density of the planar magnets, which contributes to power density improvement. Design method and calculation process of such split planar resonant inductor are provided. To verify the feasibility of the proposed design method, a 1 kV/ 48 V 6.6 kW, 210 kHz SiC LLC prototype was built, and the experimental results are given.

Key words: SiC; LLC converter; split resonant tank; design method; interleaved winding connecting scheme

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0 Introduction

With the development of SiC MOSFET, 1 kV bus voltage is availiable to reduce the current and thus reduce the loss of bus[1]. Recent years, lots of effort is made on logical link control (LLC) converter in high voltage situation. A 800 V input 28 V/ 2 kW three-level converter is proposed in Ref.[2], but three-level topology need more switching components, which has low reliability compared with 2-level topology. A 800 V input and 500 W output LLC converter is presented in Ref.[3]. A 380 V input 6.6 kW output on-board charger is present in Refs.[4-5]. However, in cases as tethered drones, 1 kV input voltage and over 4 kW power is prefered, so further work needs to be done in such applications.

LLC converters with the split resonant tanks provide solution. A 1 kV input and 4 kW output LLC converter is presented in Refs.[6-8]. Since 140 ns switching time of SiC induced high dv/dt of 11.8 kV/ μs at 1 kV input stage, large displacement current emerges through the parasitic capacitance of planar transformers, which distorts the resonant current and breaks the zero voltage switching (ZVS) condition. Split resonant tank provides symmetrical resonant current by symmetrical impedance, and improves distortion of resonant current. However, no design method of the planar inductor in such split resonant tank is proposed .

This paper proposes a method to design such split resonant inductor in LLC converter. Besides, an interleaved winding connecting scheme is proposed to further improve the power density. The key point is to increase the utilization of the winding connectors, decrease the number of connectors on each print circuit board (PCB), and reduce the quantity of clearances between connectors. With the interleaved winding connecting scheme, the converter power density rises from 63.4 W/ in^3[7] to

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93.59 W/in^3. The method for realizing such connecting scheme is provided in this paper either.

1 Inductor Parameter Design

1.1 Design of resonant parameters

Fig. 1 is the topology of the LLC converter with split resonant tanks. Planar magnets are adopted owing to low profile, good thermal characteristic and ease of manufacturability[9-10]. The input voltage varies from 900 V to 1 kV, and the output is 48 V/6.6 kW, thus high ratio transformer is needed. To improve the thermal performance and reduce the height of the whole converter[11-13], matrix transformer is adopted, and the transform ratio of single transformer N is calculated as

$$N=\frac{V_{\text{in}}}{n_{\text{tr}}V_{\text{o}}} \tag{1}$$

where n_{tr} is the number of transformer, V_{in} the input voltage, and V_{o} the output voltage.

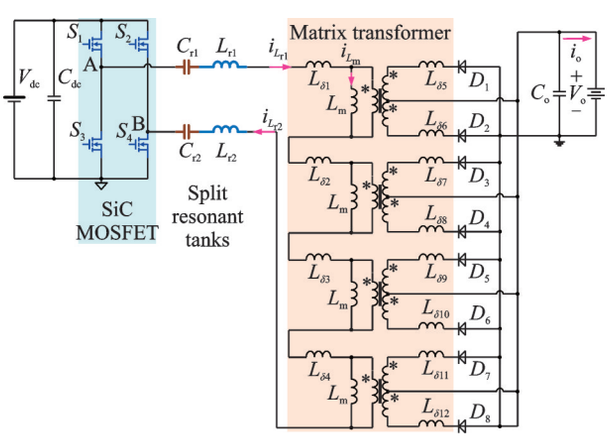


Fig.1 LLC converter with split resonant tanks

Since the transform ratio of single transformer N is decided, the maximum gain can be calculated as 1.1 when the input voltage is 900 V, and the minimum gain can be calculated as 1.0 when the input voltage is 1 kV.

According to first harmonic analysis (FHA), the DC gain G_{dc} of the converter and the resonant parameters can be calculated as

$$G_{\text{dc}}=\frac{1}{\sqrt{\left[1+\frac{1}{\lambda}\left(1-\left(\frac{1}{f_{\text{n}}}\right)^2\right)\right]^2+\left(f_{\text{n}}-\frac{1}{f_{\text{n}}}\right)^2Q^2}} \tag{2}$$

$$f_{\text{n}}=\frac{f_{\text{s}}}{f_{\text{r}}} \tag{3}$$

$$f_{\text{r}}=\frac{1}{2\pi\sqrt{L_{\text{r}}C_{\text{r}}}} \tag{4}$$

$$\lambda=\frac{L_{\text{m}}}{L_{\text{r}}} \tag{5}$$

$$R_{\text{ac}}=\frac{8(n_{\text{tr}}N)^2}{\pi^2}\frac{V_{\text{o}}}{I_{\text{o}}} \tag{6}$$

$$Q=\frac{1}{R_{\text{ac}}}\sqrt{\frac{L_{\text{r}}}{C_{\text{r}}}} \tag{7}$$

where λ is the inductance ratio, Q the quality factor, f_{n} the normalized frequency, f_{s} the switching frequency, f_{r} the resonant frequency, L_{r} the resonant inductance, C_{r} the resonant capacitance, L_{m} the magnetizing inductance, and R_{ac} the equivalent resistance of load.

To make a compromise between the power density and the efficiency of the whole module, 210 kHz is chosen as the resonant frequency. It needs to be mentioned that it is tricky to determine the inductance ratio λ and quality factor Q in such 1 kV input, 6.6 kW output situation. Compromise needs to be made between efficiency and the gain. According to Eq.(7), large Q results large C_{r} and L_{r}, thus results small resonant current, which helps to reduce the conduction loss of MOSFET and the copper loss on primary side of magnets. However, with large Q (e.g. $Q=1.2$), when input voltage is 900 V, the DC gain of the converter cannot meet the output voltage requirement, as the red curve shown in Fig.2(a). It is the same when refers to the inductance ratio λ. Large λ (e.g. $\lambda=5.0$) results large L_{m}, thus results small primary current, at the sacrifice of maximum gain, as the red curve shown in Fig.2(b). In order to obtain enough DC gain, iterative process needs to be done until the DC gain fulfills the requirment of input voltage. For example, $\lambda=5$ is chosen, then Q is decided according to

$$Q=\frac{1}{\lambda M_{\text{max}}}\sqrt{\lambda+\frac{M_{\text{max}}{}^2}{M_{\text{max}}{}^2-1}} \tag{8}$$

where M_{max} is the maximum gain of the converter. Q is calculated as 0.596. With the DC gain curve, it is obvious that the DC gain cannot fulfill the requirement when the input voltage is 900 V. Then the process repeats, which means $\lambda=4$ is chosen, and Q is

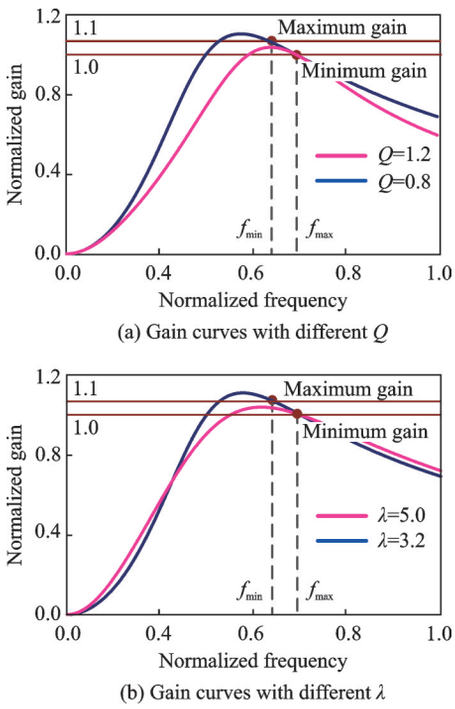


Fig.2 Gain curve of LLC converter

calculated as 0.71, however the DC gain cannot fulfill the requirement when the input voltage is 900 V either. Finally, $Q=0.8$ and $\lambda=3.2$ are chosen, since such parameters compromise between regulation capability[14] and the efficiency.

As analyzed before, resonant parameters are calculated as follows: the transform ratio N is chosen as 5∶1; the magnetic inductance L_m is chosen as 230 μH, considering four matrix transformers are used, 57 μH for each; the resonant inductance L_r is chosen as 72 μH, considering leakage inductance of transformers is about 1.5 μH and split inductor is used, 33.5 μH for each resonant inductor; the resonant capacitance C_r is chosen as 8 nF, considering split resonant tank is used, 4 nF for each resonant tank. Since the input voltage varies from 900 V to 1 kV, switching frequency changes from 179 kHz to 210 kHz. In order to guarantee ZVS of MOSFET in primary side and ZCS of diode in second side, the converter will work at the resonant frequency when the input voltage is 1 kV.

1.2 Design of the split resonant inductor

As the resonant parameters set, resonant inductor can be designed through faradays law[15] With a compromise made between the height and footprint. PQ32/25 with DMR95 material by DEMEGC is chosen as the core of inductor, thus the effective area of core $A_{e\_L_r}$ is 153.1 mm^2. In order to avoid saturation of core, the maximum flux $B_{m\_L_r}$ is chosen as 187.2 mT. The inductor turns can be calculated through faradays law

$$N_{L_r}=\frac{L_r}{2}\frac{i_{L_r\_max}}{2B_{m\_L_r}A_{e\_L_r}} \tag{9}$$

where N_{L_r} is the inductor turn number, and L_r is the resonant inductance. Since split resonant tank is used, each inductor is $L_r/2$. $i_{L_r\_max}$ is the peak value of resonant current and the specified value can be obtained through simulation. $B_{m\_L_r}$ is the maximum flux and $A_{e\_L_r}$ is the effective area of core.

2 Interleaved Winding Connecting Scheme

From the equations before, N_{L_r} is calculated as 12. However, when it comes to planar magnets, such turn number N_{L_r} will cause large footprint of PCB winding, considering about the clearance between winding connectors for 1 kV application.

For example, 4-layer PCB is used to realize the 12-turn inductor, and one PCB is used as two turns in series through one group of vias, that means regarding the top layer and the signal layer 1 in parallel as the 1st turn, the signal layer 2 and the bottom layer in parallel as the 2nd turn. In other words, six pieces of PCB in series are needed to connect through half holes on each PCB.

Followings are traditional winding connecting scheme and the proposed interleaved scheme to realize six pieces of PCB in series. As shown in Fig.3 (a), with traditional scheme, seven half holes in each PCB is necessary. Considering about the clearances for 1 kV between half holes, large footprint of the winding is needed. Since the volume of PCB winding equals the footprint multiplies height, large footprint of the winding makes the inductor bulky.

From Fig.3(a), the problem is that, half holes in red are totally wasted. As shown in Fig.3(b), if the connections go interleaved way, half holes in red can be fully used. In this way, only three or four

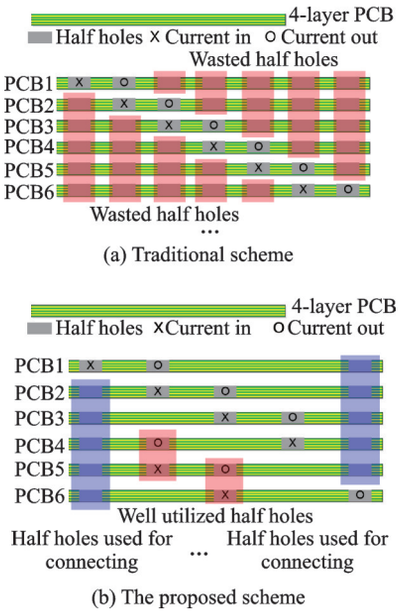


Fig.3 Comparison of winding connecting schemes

half holes in each PCB will be needed, thus the footprint of PCB winding will shrink, and the volume of the inductor will significantly decreases. It should be noted that, half holes in blue, are used for connecting.

Moreover, arbitrary number of PCB can be connected without adding half holes by continuing the interleaved connection. Since it changes the connecting scheme only, this method can be generalized to all of the magnets which have large number of turns.

3 Comparison of PCB Layout in Traditional Winding Connecting Scheme and Interleaved Scheme

In order to show the footprint reduction directly, comparison of the PCB layout in traditional winding connecting scheme and the proposed scheme is made, as shown in Fig.4. In order to ensure fair comparison, both schemes use 12 pieces of 4-layer PCB to realize 12 turns inductor, both layouts have the same 1.7 mm terminal clearance for 1 kV, both layouts are the same except for the terminal part (showed in red), both layouts have the 32 mm limitation of width due to the application and both layouts are designed with the same core size (PQ32/25).

Fig.4(a) shows the PCB layout in traditional winding connecting scheme. Since the layout width is limited, it is impractical to use seven half holes to connect six pieces of PCB in series and regard one PCB as two turns. The better choice is using five half holes to connect four pieces of PCB in series and regarding one PCB as three turns. That means regarding the top layer as the 1st turn, two signal layers in parallel as the 2nd turn, and the bottom layer as the 3rd turn, so two groups of via in each PCB are needed.

Fig.4(b) shows the PCB layout in the proposed winding connecting scheme. Since arbitrary number of PCBs is connected with only three or four half holes in each PCB, connecting six pieces of PCB in series and regarding one PCB as two turns, is practical. That means regarding the top layer and signal layer1 in parallel as the 1st turn, the signal layer 2 and the bottom layer in parallel as the 2nd turn, thus only one group of via in each PCB is needed.

From Fig.4, length of the winding reduces from 35 mm to 29 mm, since the quantity of clearances for 1 kV reduces from four to one. The footprint of the PCB winding and the volume of the

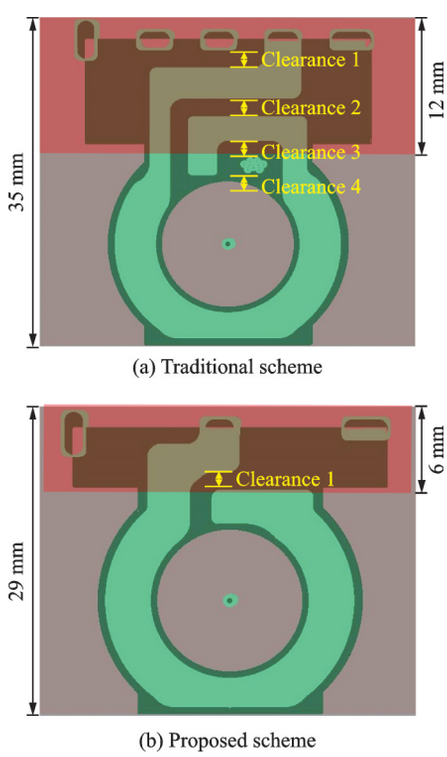


Fig.4 Comparison of PCB footprint

whole inductor reduce 17.14%. In addition, the terminal length decreases 50% from 12 mm to 6 mm, which will cause almost 50% terminal resistance reduction.

4 Winding Arrangement of Proposed Inductor

With the interleaved connecting scheme, the winding arrangement is shown in Fig. 5. As mentioned before, one piece of 4-layer PCB is regarded as two turns in series. Since the window height is 14 mm, 12 pieces of 1 mm PCB is used. As discussed before, six pieces of PCB can be connected in series without adding footprint of PCB, so PCB1—PCB6 in series are used to realize 12 turns of inductor winding, and PCB7—PCB12 are in parallel with PCB1—PCB6.

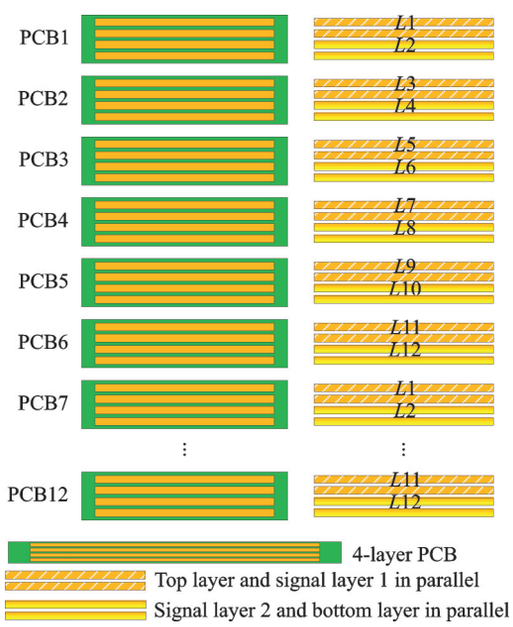


Fig.5 Winding arrangement of the proposed inductor

5 Comparison of Parameters in Traditional Winding Connecting Scheme and Interleaved Scheme

As mentioned above, with the interleaved connecting scheme, the terminal length of PCB wire decreases 50% from 12 mm to 6 mm, which will cause almost 50% terminal resistance reduction. To show difference of parameter between traditional winding connecting scheme and the interleaved scheme, finite element analysis (FEA) simulation is made by ANSYS, as shown in Fig.6.

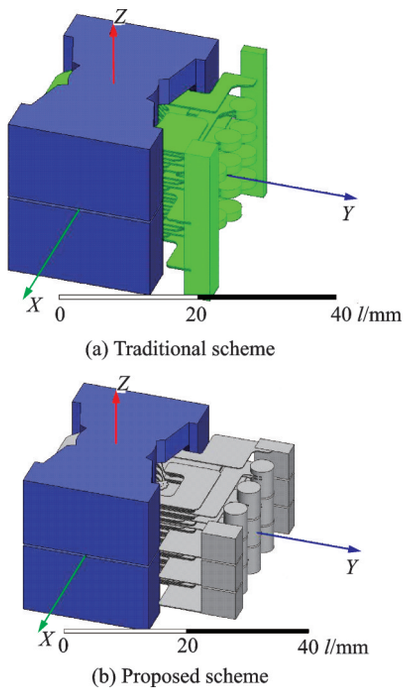


Fig.6 FEA simulation models

Table 1 shows the results of FEA simulation. The proposed scheme decreases the AC resistance by 24.15%, without changing the inductance. It is worth mentioning that the reduction of AC resistance means the reduction of copper loss, which contributes to the efficiency of the converter.

Table 1 FEA simulation results

Scheme	AC resistance/mΩ	Inductance/μH
Traditional scheme	8.07	33.56
The interleaved scheme	6.12	33.42

6 Exprimental Results

In order to verify the validity of the design method mentioned above, a 1 kV input, 48 V output, 6.6 kW, SiC LLC prototype with the proposed split resonant inductor is built. The topology is shown in Fig.1. And the parameters of the convertor are shown in Table 2. The resonant tank is composed of four matrix transformers (each transformer has L_m of 59 μH), two resonant inductors (each has inductance of 33 μH) and 32 resonant capacitors

(each has capacitance of 1 nF), that is to say, since RMS of primary current is 9.3 A, to reduce the ESR of capacitors, 16 capacitors in one group are in parallel, and two groups of capacitors are in series. Main components used in the power stage are listed in Table 3.

Table 2 Key parameters of the prototype

Parameter	Value
Resonant frequency f_r/ kHz	210
Transformer	N=5∶1, L_m=236 μH
L_r /μH	67
C_r/ nF	8
Input voltage/ V	900—1 000
Output voltage/ V	48
Total power/ kW	6.6

Table 3 Power stage components

Name	Part number
C_{in}	2220Y1K50154KXTWS2, 1.5 kV, 0.15 μF×6 (Knowles) B32024A3224M000, 1.5 kV, 0.22 μF×3 (TDK)
L_{r1}, L_{r2}	PQ 32/25, DMR95 (DMEGC)
C_{r1}, C_{r2}	C1812C102JGGACTU, 2 kV, 1 nF×16 (KEMET)
C_o	KCM55WR72A226MH01L, 100 V, 22 μF×30 (Murata) GCM32DC72A475ME02L, 100 V, 4.7 μF×16 (Murata)
T_r	PQI 35/23, DMR96 (DMEGC)
Q_1—Q_4	C3M0075120K 1.2 kV, 30 A (Cree)

Fig.7 shows the photographs of the prototype. With the help of the interleaved winding connecting scheme, the dimensions of the prototype are 215 mm×215 mm×25 mm, thus the power density is 93.59 W/ in^3. Fig.8 shows the proposed split planar resonant inductor. Two same inductors are used to realize the split resonant tank and the symmetrical impedance. The core size is PQ32/25 and the material is DMR95 produced by DMEGC as mentioned above. From the front view in Fig.8(a), it can be seen how these PCB windings connect with each other.

Fig.9 shows the key waveforms of the prototype at 6.6 kW load under close-loop condition.

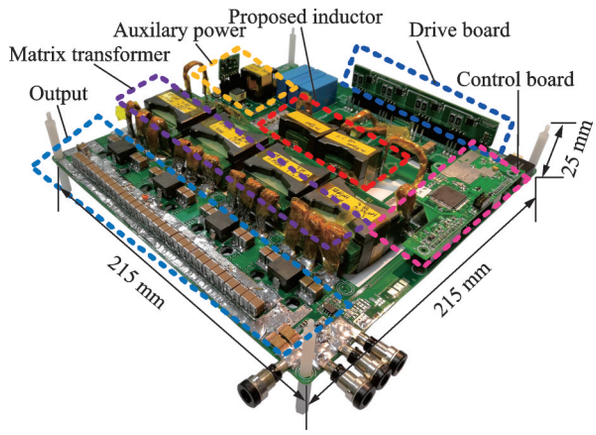
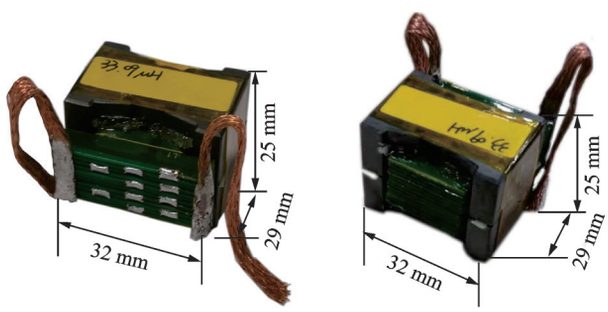
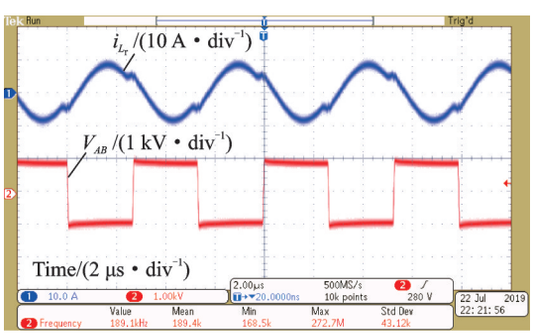


Fig.7 Photo of prototype

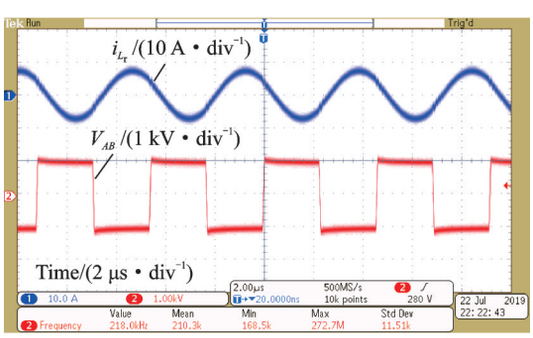


(a) Front view (b) Back view

Fig.8 Photoes of resonant inductor



(a) 900 V input and 6.6 kW load



(b) 1 kV input and 6.6 kW load

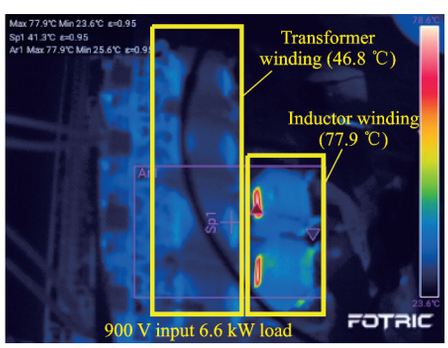
Fig.9 Key waveforms

These waveforms show that the converter is able to work stably with the proposed inductor. The blue curve is the resonant current, and the red curve is

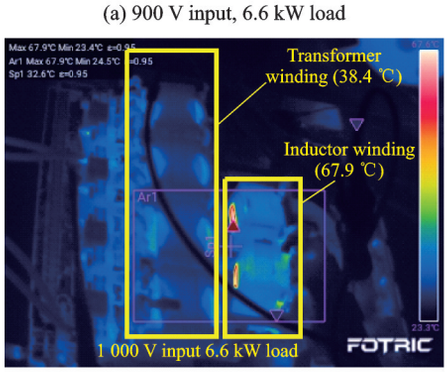
the input voltage of the resonant tank. When the input voltage rises from 900 V to 1 kV, the switching frequency rises from 189 kHz to 210 kHz. From Fig. 9(a), current waveform when $f_s < f_r$ can be seen, and from Fig. 9(b), current waveform at the resonant frequency can be seen, which are consistent with the design before.

Fig. 10 shows the thermal images of the prototype. It is needed to be mentioned that fan 3258 J/2 HHP produced by EMBPAPST is used. The output power of this fan is 24.3 W, and the speed is 6 650 r/min. From the thermal images the hottest part of the prototype is the inductor winding, the temperature is 77.9 ℃ at 900 V input and 67.9 ℃ at 1 kV input. Since input power is almost fixed, when the input voltage is 900 V, current on primary side is larger compared with situation when the input voltage is 1 kV. Large current results in high temperature on the winding of the magnet components.

Fig. 11 shows the waveforms under soft-start condition. These waveform shows that the converter is able to work stably with the proposed split planar inductor under soft-start condition. The blue curve is the resonant current, the red curve is the input voltage of the resonant tank, and the green curve is the output voltage. The soft-start process comprises three stages: phase shift (to increase the equivalent duty cycle), deadtime regulation (to prevent the converter from short-circuit condition) and frequency regulation (let PI controller calculate the frequency needed to realize accurate DC gain). The soft-start process is controlled by DSP TMS320F28374SPZP (from Texas Instrument). Different slope rates can be seen in the green curve, which demonstrates different stages in the soft-start procedure.

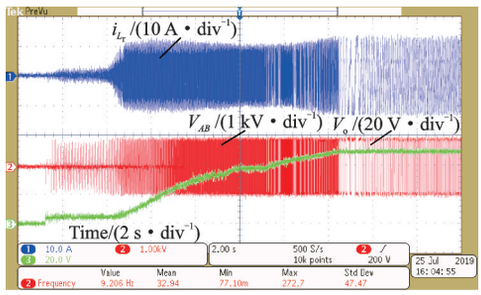


(a) 900 V input, 6.6 kW load

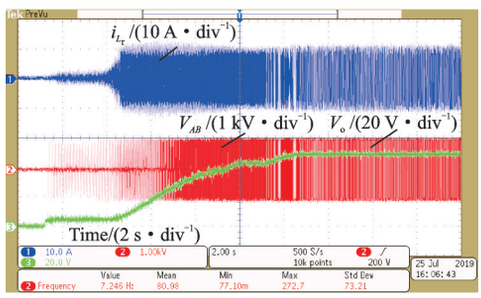


(b) 1 kV input, 6.6 kW load

Fig.10 Thermal images



(a) 900 V input, 6.6 kW load



(b) 1 kV input, 6.6 kW load

Fig.11 Soft start waveforms

Fig. 12 shows the efficiency curve of the prototype under close-loop condition. The brown curve in Fig. 12 shows the efficiency when the input voltage is 1 kV, and the blue curve shows the efficiency when the input voltage is 900 V. The peak efficiency on full rage load is 95.73% when the input voltage is 1 kV and the load is 4.4 kW. Since the current of 900 V input is bigger than current of 1 kV in-

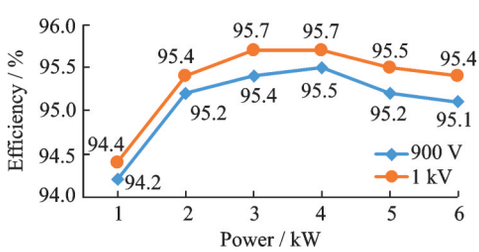


Fig.12 Efficiency curves under close-loop condition

put, higher efficiency is got when the input voltage is 1 kV.

7 Conclusions

This paper proposes a design method to design the split resonant inductors of a LLC converter, which is used in 1 kV input voltage, 48 V output voltage, 130 A output current situation. Based on such split resonant inductor, an interleaved winding connecting scheme is proposed to improve the power density. To verify the feasibility of the method and the winding connecting scheme, a 1 kV/ 48 V 6.6 kW, 210 kHz SiC LLC prototype with the split resonant inductor is built. Experimental results and measurements show that, with the proposed design method, the power density of the prototype is 93.59 W/in^3 and the peak efficiency is 95.73%.

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