Characterization of Self-driven Cascode-Configuration Synchronous Rectifiers

*REN Xiaoyong**, *LI Kunqi*, *CHEN Qianhong*

Aero-Power Sci-Tech Center, College of Automation Engineering, Nanjing University of Aeronautics and Astronautics, Nanjing 210016, P. R. China

(Received 15 August 2019; revised 3 December 2019; accepted 10 December 2019)

Abstract: This paper presents a cascode configuration synchronous rectifier device based on silicon MOSFET and Schottky diode, which can replace traditional power diode directly. This structure has self-driven ability with simple external circuit, and the conduction characteristic is preferable to a power diode. Static characterization and switching behavior analysis of proposed structure are conducted in this paper. The switching process is illustrated in detail using real model which considers the parasitic inductances and the nonlinearity of junction capacitors. The real time internal voltage and current value during switching transition are deduced with the equivalent circuit. To validate the analysis, two voltage specification rectifiers are built. Finally, double-pulse test results and the practical design example verify the performance advantages of proposed structure.

Key words: synchronous rectifier (SR); self-driven; cascode structure; power diode

CLC number: TM461 **Document code**: A **Article ID**: 1005-1120(2019)06-0902-10

0 Introduction

Synchronous rectifiers (SR) technology is an important method to improve converter efficiency, in which power MOSFETs take the place of diode as the rectifier to reduce conduction losses[1-4]. Generally there are two types of driving methods: external-controlled methods and self-driven methods. Self-driven methods develop a SR driving signal from the voltage signal, which exists in the switching topology and coincides with the desired drive timing[5-9]. It is simple and effective, however some topologies such as LLC resonant converter can hardly realize self-driven[10-11]. Therefore, external driving signals are generated by detecting either the current through the field effect transistor (FET) or the voltage drop across the FET[10-16]. Though it works well, the driver, the sampling and signal processing circuit increase the cost and complexity of the system.

In order to realize simple driver of SR, some new methods of self-driven SR based cascode structure which use SiC JFET and Si MOSFETs cascode with Si Schottky diode have been researched[17]. It is used to replace front-end rectifier diode. Compared to the traditional external self-driver method, it is more effective and cheaper. But the additional circuit of this structure also has more components, which means it is hard to integrate all components in one package.

This paper presents a cascode structure self-driven rectifier with simplified additional driver circuit, which is called active diode (ACD). This structure can realize integrated package just like cascode GaN FET[18], which means it can replace power diode directly. Both static and transient characteristics of the proposed ACD are analyzed in detail, such as the forward conduction and reverse breakdown characteristic, and turn-on and turn-off transient processes. This paper is organized as follows: Section 1 describes the basic structure and static characteristic of ACD. The forward characteristics

*Corresponding author, E-mail address: renxy@nuaa.edu.cn.

How to cite this article: REN Xiaoyong, LI Kunqi, CHEN Qianhong. Characterization of Self-driven Cascode-Configuration Synchronous Rectifiers[J]. Transactions of Nanjing University of Aeronautics and Astronautics, 2019,36(6):902-911.
http://dx.doi.org/10.16356/j.1005-1120.2019.06.003

of different combinations are compared with traditional power diode in order to highlight the advantage of this structure; Section 2 analyzes the detailed switching process, reverse voltage distribution and the expressions of voltage and current at ACD during switching transition; Section 3 verifies the proposed structure with experimental results. Finally, some conclusions are outlined in Section 4.

1 Basic Structure and Static Characteristic of ACD

The structure of the proposed ACD is shown in Fig.1, which consists of MOSFET S_1 and Schottky diode D_1. In this structure, D_1 is in series with S_1 to achieve the function of power diode. The cathode and anode terminals of the module are S_1 drain terminal and D_1 anode terminal, respectively. Bias capacitor C_c is connected to the S_1 gate terminal and D_1 anode terminal to provide S_1 driving voltage. Transient voltage suppressor diodes D_{Z1} and D_{Z2} are in parallel with S_1 gate and source terminal to protect the S_1 gate from overvoltage and spikes. Compared to the fast recovery diode, Schottky diodes do not have reverse recovery period. Therefore in this structure D_1 usually uses Schottky diode to get the better dynamic performance.

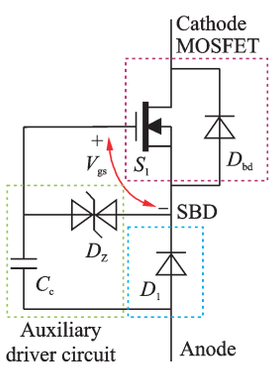


Fig.1 Basic structure and comportment of ACD

In the turn-off state, S_1 and D_1 sustain reverse voltage in series. Voltage distribution between two components is decided by turn-off transition process, which will be analyzed in next section. The peak repetitive reverse voltage of ACD V_{RRM_ACD} is the total of the breakdown voltages of both D_1 and S_1 when the parameter is very well matched, such as

$$V_{RRM\_ACD} = V_{RRM\_D1} + V_{(BR)DSS\_S1} \tag{1}$$

where V_{RRM_D1} is peak repetitive reverse voltage of D_1 and $V_{(BR)DSS\_S1}$ is drain-source breakdown voltage of S_1. Usually the parameter of ACD can hardly be matched perfectly, therefore V_{RRM_ACD} is definitely less than the sum of two reverse voltage as shown in Eq.(1).

In the turn-on state, V_{gs} is equal to V_c (ignore the voltage drop of D_1). Forward current flows through the diode and MOSFET channel, the maximum forward current of ACD is the smaller one of D_1 maximum average forward current and S_1 continuous drain current, such as

$$I_{F(av)\_ACD} = \min\left[I_{F(av)\_D_1} \quad I_{D\_S_1} \right] \tag{2}$$

The ACD forward voltage drop consists of the D_1 forward voltage drop $V_{f\_D_1}$ and the S_1 on state resistance R_{ds_on}, the relationship with current is

$$V_{f\_ACD}(i_f) = V_{f\_D_1}(i_f) + i_f \times R_{ds\_on} \tag{3}$$

where i_f is the forward current of ACD. The typical forward characteristic of ACD and two discrete devices are shown in Fig.2. With the forward current increasing, S_1 forward voltage drop increases linearly from zero, while D_1 forward voltage drop increases nonlinearly from an initial voltage. From Fig.2, it can be noted that, with respect to the forward current, the derivative of the S_1 forward voltage is larger than that of D_1, leading to a crossover point in the figure. That is, before the crossover point, D_1 dominates the forward voltage drop. With the forward current further increasing, S_1 dominates the forward voltage drop, which makes the forward voltage of ACD has an approximately linear relationship with the forward current.

Based on the aforementioned analysis, the for-

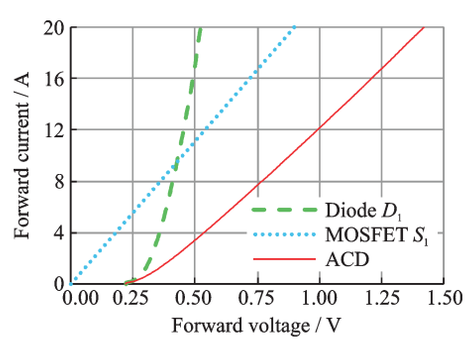


Fig.2 Forward characteristic of MOSFET, diode and ACD

ward voltage drop of ACD is determined by S_1 and D_1. There are different combinations of S_1 and D_1 to construct the ACD with given specifications. In order to achieve better forward characteristics, it is necessary to find the optimal combination. In this section, two different specification power diodes are chosen to investigate the combination principle for better conduction performance.

Two popular voltage ratings are chosen to be evaluated. The first voltage specification type is a high voltage which V_{RRM_ACD}=650 V. There are two combination types to realize this: 600 V silicon carbide Schottky barrier diode (SiC SBD) cascaded with 55 V MOSFET or 60 V silicon Schottky barrier diode (Si SBD) cascaded with 600 V MOSFET. The forward characteristic of these two types and traditional power diode are shown in Fig.3. It is obvious that 600 V MOS cascaded with 60 V Si SBD has better conduction characteristic.

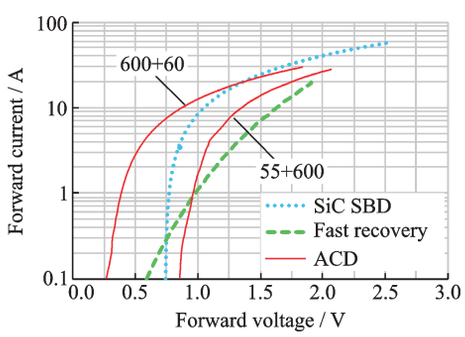


Fig.3 Forward characteristic comparison of two types of ACD with SiC SBD and fast recovery diode in 650 V

The second voltage specification type is a low voltage which V_{RRM_ACD}=200 V. There are a variety of voltage specification devices to realize such combination. The forward characteristics of four typical combination types and traditional power diode are shown in Fig.4.

As can be seen in Fig.4, the lower the MOSFET voltage level is, the higher ACD forward voltage drop will be. Therefore, MOSFET voltage rating approaching the ACD voltage rating is preferred for better forward performance. Such a combination can also achieve low threshold voltage and dynamic resistance besides the excellent forward characteristics.

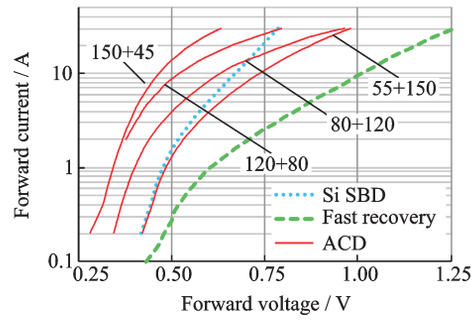


Fig.4 Forward characteristic comparison of four types of ACD with 150 V Si SBD and fast recovery diode

2 Analysis of Switching Behavior and Dynamic Characteristic

In this section, the detailed ACD switching mode analysis is presented based on the double pulse test (DPT) together with simulation results. The test setup is shown in Fig.5. To accurately measure forward current i_f, the device-under-test (DUT) and inductive load L_f are placed at the low side. The proposed analytical model includes the most parasitic parameters in actual device: parasitic inductors and capacitors. The symbol and reference direction of current and voltage are also marked in Fig.5.

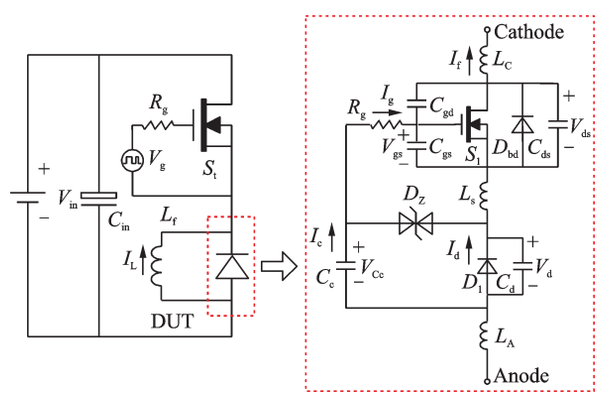


Fig.5 Simulation circuit and analysis module of ACD

2.1 ACD turn-off transition switching behavior and voltage distribution

The voltage distribution between S_1 and D_1 is very important, which determines the reliability of proposed ACD. It is necessary to analyze the turn-off transition and find the relationship of V_d and V_{ds}.

The key waveforms during turn-off transition are shown in Fig.6. Before S_t turns on, the induc-

tive load current I_L transfers from ACD to S_1, i_f decreases linearly and the slope depends on the value of R_g. When i_f decreases to zero, the turn-off transition begins. This transition can be divided into four stages. The detailed analysis is given in the following part.

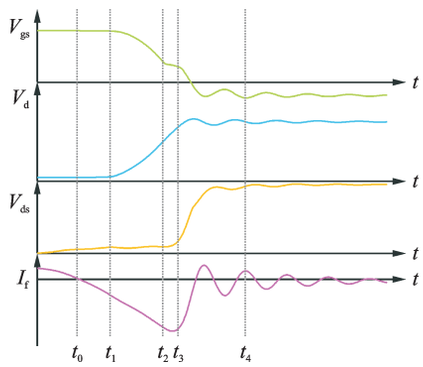


Fig.6 Key waveforms of ACD during turn-off transition

(1) Stage I: Diode reverse recovery delay period $[t_0, t_1]$

After i_f decreases to zero at t_0, diode D_1 can hardly turn off immediately due to the energy storage effect of PN junction. During this period, diode current reversely increases to discharge D_1 junction energy. Therefore, S_1 and D_1 are entire conduction (as shown in Fig.7), the forward current i_f, which equals to i_d, reversely increases with the same slope of that before t_0. Since D_1 uses Schottky diode in this structure normally, the reverse recovery process is usually around a few nanoseconds. This period ends when diode reverse recovery process finishes at t_1.

(2) Stage II: Diode turns-off and MOSFET gate driver delay period $[t_1, t_2]$

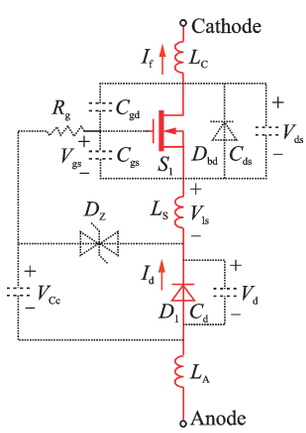


Fig.7 Equivalent circuit of ACD during turn-off stage I

When reverse recovery process finishes at t_1, D_1 turns off and i_d flows through the junction capacitor C_d to charge it, then the reverse voltage of D_1, V_d increases. Due to gate capacitor C_{gs} of S_1, V_{gs} will be still higher than miller voltage, S_1 keeps on in this period (as shown in Fig.8). The Kirchhoff voltage equation for this circuit is given below, which are composed of C_c, C_{gs}, C_d and L_s

$$V_d + V_{ls} = V_c - V_{gs} \tag{4}$$

Due to tiny parasitic inductance L_s, V_{ls} is negligible. With the S_1 driving voltage V_{gs} decreasing at this period, V_d increases. Accordingly, i_g flows through C_{gs} and C_c in single circuit path. Above is the self-driven mechanism of this structure. To analyze this period equivalent circuit in complex frequency domain, the equations are expressed as follow

$$\begin{cases} V_g(s) = i_g(s) * \left(\dfrac{1}{sC_{iss}} + \dfrac{1}{sC_c} + R_g\right) \\ V_d(s) = i_d(s) * \left(sL_s + \dfrac{1}{sC_d}\right) - L_s i_f(t_1) \\ i_f(s) = i_g(s) + i_d(s) \\ i_f(s) = \dfrac{k_{if}}{s^2} + \dfrac{i_f(t_1)}{s} \end{cases} \tag{5}$$

In this period, i_f reversely increases with the same slope in stage I as S_1 still conducts. After solving Eq.(5), $i_g(s)$ and $i_d(s)$ are

$$i_g(s) = \frac{as^2 + C_{iss}C_c}{as^2 + bs + c} \cdot i_f(s) - \frac{asi_d(t_1)}{as^2 + bs + c} \tag{6}$$

$$i_d(s) = \frac{bs^2 + (c - C_{iss}C_c)}{as^2 + bs + c} \cdot i_f(s) + \frac{asi_d(t_1)}{as^2 + bs + c} \tag{7}$$

where $a = C_{iss}C_cC_dL_s$, $b = C_{iss}C_CC_dR_g$, $c = C_{iss}C_c + C_{iss}C_d + C_cC_d$. With the help of Generalized Ohm's law, the voltage expression of this circuit can be found then. This period ends when V_{gs} drops to the miller voltage at t_2.

(3) Stage III: Main transition period $[t_2, t_3]$

When $t = t_2$, V_{gs} decreases to the miller platform, the operation state of MOSFET channel transits from the saturation-on state to linear state. The channel current i_{CH} is determined by V_{gs}. With V_{gs} decreasing, i_{CH} will decrease either. Then the excess forward current flows through C_{ds} to charge it. Therefore, the voltage V_{ds} increases. The equivalent circuit of this stage is shown in Fig.9 and the current flowing through ACD satisfies

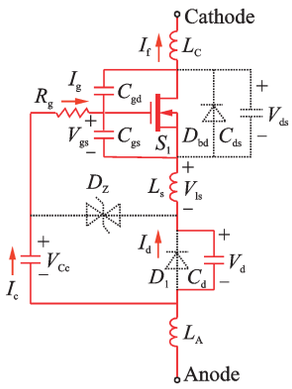


Fig.8 Equivalent circuit of ACD during turn-off stage II

$$i_f = i_{gd} + i_{gs} + i_{CH} + i_{ds} \tag{8}$$

Since C_{gd} is much smaller than C_{ds} for most types of MOSFET, i_{gd} is much smaller than i_{ds} which causes the voltage change of two capacitors is nearly same during this period. To simplify the analysis, i_{gd} is ignored in following analysis. The complex frequency domain equations at this period are

$$\begin{cases} V_d(s) = i_g(s) \cdot \left(\dfrac{1}{sC_{gs}} + \dfrac{1}{sC_c} + R_g\right) \\ V_d(s) = i_d(s) \cdot \left(sL_s + \dfrac{1}{sC_d}\right) - L_s i_f(t_2) \\ i_f(s) = i_g(s) + i_d(s) \\ i_f(s) = \dfrac{k_{if}}{s^2} + \dfrac{i_f(t_1)}{s} \end{cases} \tag{9}$$

In this stage, the channel of MOSFET is in linear on state, and i_f increases with almost the same slope as in stage II. After solving Eq.(9), $i_g(s)$ and $i_d(s)$ can be expressed as follows

$$i_g(s) = \frac{as^2 + C_{gs}C_c}{as^2 + bs + c} \cdot i_f(s) - \frac{asi_d(t_1)}{as^2 + bs + c} \tag{10}$$

$$i_d(s) = \frac{bs + (c - C_{gs}C_c)}{as^2 + bs + c} \cdot i_f(s) + \frac{asi_d(t_1)}{as^2 + bs + c} \tag{11}$$

where $a = C_{gs}C_cC_dL_s$, $b = C_{gs}C_CC_dR_g$, $c = C_{gs}C_c + C_{gs}C_d + C_cC_d$. According to the time domain analysis, the voltage and current of this circuit can be expressed as

$$\begin{cases} V_d(t) = \int i_d(t)/C_d \mathrm{d}t \\ V_{gs}(t) = \int i_d(t)/C_{gs} \mathrm{d}t \\ i_{ch}(t) = g_{fs} \cdot (V_{gs}(t) - V_{th}) \\ i_{ds}(t) = i_f(t) - i_{CH} \\ V_{ds}(t) = \int i_{ds}(t)/C_{ds} \mathrm{d}t \end{cases} \tag{12}$$

According to Eqs.(10)—(12), the time domain expression of $V_d(t)$ and $V_{gs}(t)$ can be found. Therefore $V_{ds}(t)$ can also be deduced with KVL equation. In this stage, i_{ch} continuously decreases with V_{gs} decreasing. When i_{ch} decreases to zero at t_3, which presumes that V_{gs} decreases below the S_1 threshold voltage, the channel of MOSFET is cutoff and this stage ends.

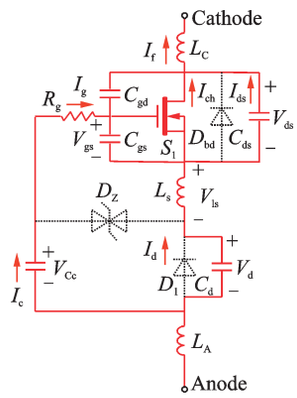


Fig.9 Equivalent circuit of ACD during turn-off stage III

(4) Stage IV: Remaining transition period $[t_3, t_4]$

At t_3, V_{gs} decreases below V_{th} and S_1 channel is cut off. All S_1 current flows into C_{ds} patch and charges it (as shown in Fig.10). In this period, all forward current i_f discharges parasitic capacitor for ACD. The expression of i_f is

$$\frac{V_{ac_{t3}}}{s} = i_f(s) * Z + \frac{V_{d_{t3}} + V_{ds_{t3}}}{s} - s(L_C + L_A) * i_{f\_t3} - sL_s i_{d\_t3} \tag{13}$$

where Z is the equivalent complex impedance of ACD in this period, which can be expressed as

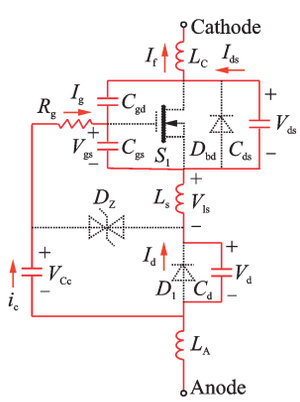


Fig.10 Equivalent circuit of ACD during turn-off stage IV

$$Z = S(L_C + L_A) + \frac{1}{sC_{ds}} + \left(\frac{1}{sC_{gs}} + R_g + \frac{1}{sC_c}\right) \Bigg\| \left(sL_s + \frac{1}{sC_d}\right) \tag{14}$$

According to Eq.(13), the expression of $i_f(s)$ in this period can be deduced. Then the expression of V_{ds}, V_d and V_{gs} can be found from Eqs.(10)—(12). This period ends when V_{ca} equals to V_{in} at t_4, and the whole turn-off transition finishes.

2.2 ACD turn-on transition switching behavior

Before the ACD turns on, the current through ACD is zero, and the voltage of ACD is V_{in}. The turn-on transition can also be divided into four stages, and the key waveforms of turn-on period are shown in Fig.11.

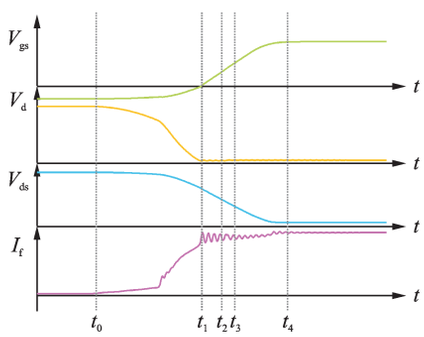


Fig.11 Key waveform of ACD during turn-on transition

(1) Stage I: MOSFET drain-source voltage falling period $[t_0, t_1]$

As top switch in DPT circuit begins to turn-off, the inductor current I_L transfers from S_t to the ACD and discharges C_d and C_{ds}. Then V_d and V_{ds} decrease immediately. Fig.12(a) shows the equivalent circuit of this stage. Based on the relationship in Eq.(4), V_{gs} will increase with the decrease of V_d. The circuit module of this period is the same as turn-off process stage IV, the voltage and current expression of this stage are also the same as Eqs.(9)—(12). This stage ends when V_{ds} decreases to zero.

(2) Stage II: MOSFET body diode conduction period $[t_1, t_2]$

At t_1, V_{ds} drops to zero before V_{gs} increases to the threshold value, the body diode D_{bd} of MOSFET turns on to freewheel inductor current I_L. The equivalent circuit of this stage is shown in Fig. 12(b), which is similar to turn-off stage II. Then the voltage and current expression of this stage still are the same as Eqs.(5)—(7). This stage ends when V_{gs} rises to MOSFET threshold voltage V_{gs_th} at t_2.

(3) Stage III: MOSFET current transform period $[t_2, t_3]$

When V_{gs} reaches V_{gs_th} at t_2, S_1 turns on and freewheeling current transfers from MOSFET body diode to channel. The equivalent circuit of this stage is shown in Fig.12(c). At this stage the circuit module is similar to that in the last stage, the only difference is the current transform process, which has no impact on the charge relationship of junction capacitor. Therefore, the current and voltage expression is same as last stage. This stage ends when V_{gs} rises to miller platform, which means that all the freewheeling current flows through S_1 channel.

(4) Stage IV: Diode junction capacitor discharge period $[t_3, t_4]$

When V_{gs} reaches miller platform at t_4, S_1 fully turns on, then the freewheeling current discharges diode junction capacitor C_d and V_d decreases. The equivalent circuit of this stage is shown in Fig. 12

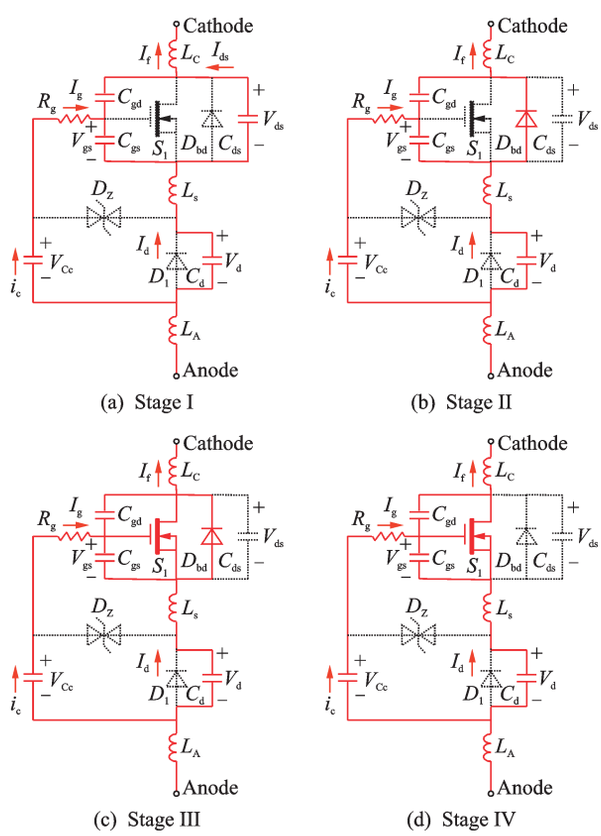


Fig.12 Equivalent circuits of ACD during turn-on stage

(d), which is still similar to that in the previous stage. Then the current and voltage expressions are the same as those in the last stage too. When V_d drops to zero, the whole turn-on transition ends and ACD transforms from turn-off state to turn-on state. After the ACD fully turns on, the inductor current I_L flows through the channel of MOSFET and diode, V_{gs} is clamped by bias capacitor voltage V_c, which maintains on state of MOSFET.

3 Experimental Results and Discussion

To verify the feasibility of proposed ACD, a double-pulse test setup is built in lab. Operation waveforms and voltage distribution are investigated. Additionally, a DC-DC prototype is also built to evaluate the performance of the proposed ACD.

3.1 Double-pulse-test waveform verification

Fig.13 shows the prototype of the double-pulse test circuit. The top switch is a high voltage silicon transistor driven with silicon-lab high performance isolated driver SI8261. The coaxial shunt resistor, which has high bandwidth and minimized parasitic inductance, is adopted to improve current measure accuracy.

Fig.14 shows the prototype of proposed ACD. Bias capacitor uses a high stability C0G material ceramic capacitor to make sure capacitance is constant under any reverse voltage and temperature. Two typical voltage-level ACDs are established to verify the voltage distribution and dynamic process in this paper.

Fig.15 shows the steady-state experimental waveforms of two kinds of ACD, which include driver voltage V_{gs}, diode reverse voltage V_d, MOSFET drain-source voltage V_{ds} and forward current i_f. The input voltages of these two ACDs are 100 V and 400 V, respectively. The average inductor current is 10 A. The experimental results show that these two ACDs can realize self-driven function, and the driver voltage V_{gs} can be clamped to a suitable value by TVS.

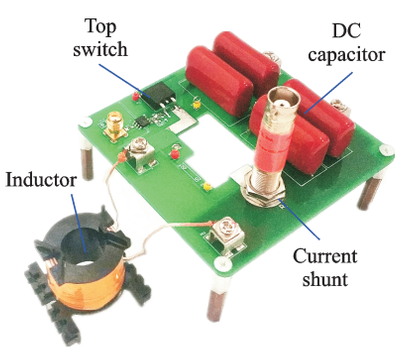


Fig.13 Prototype of double-pulse test circuit

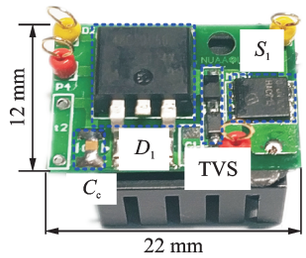
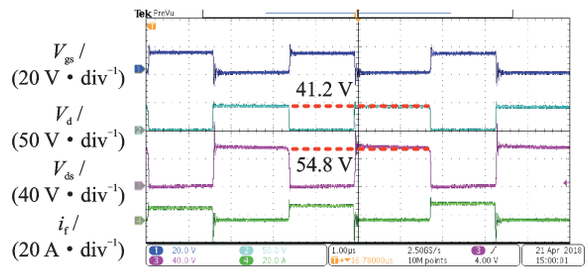
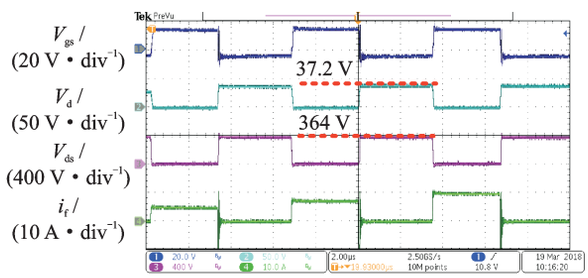


Fig.14 Prototype of ACD



(a) 150 V voltage range ACD

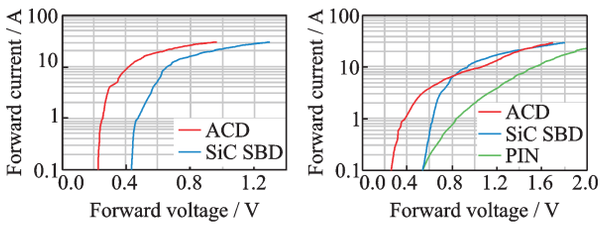


(b) 650 V voltage range ACD

Fig.15 Experimental result of double-pulse test circuit

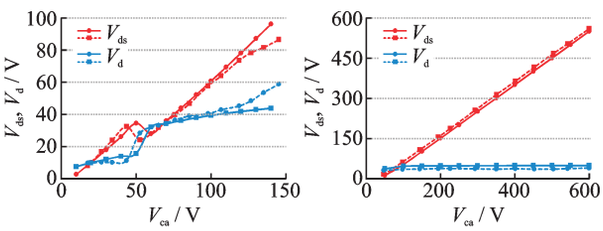
Fig.16 shows the forward characteristic of two types of ACD compared with same specification power diode by double pulse test. As can be seen, the ACD has a lower knee voltage and lower dynamic resistance. Therefore, the forward voltage drop of ACD is lower than power diode.

Fig.17 shows the voltage distribution comparison between the double-pulse test and calculated result of the proposed analytical function at Section III. Fig.17 (a) is the result of 150 V ACD and Fig.17 (b) is 650 V. The analytical function matches well with experimental results.



(a) 150 V voltage specification ACD (b) 650 V voltage specification ACD

Fig.16 Experimental result of forward characteristic by ACD and traditional diode

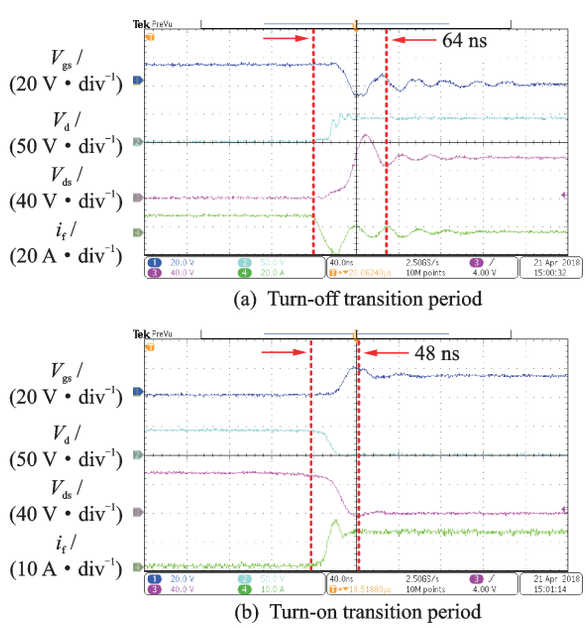


(a) 150 V voltage specification ACD (b) 650 V voltage specification ACD

Solid line: calculation result, dash line: experimental result

Fig.17 Voltage distribution comparisons

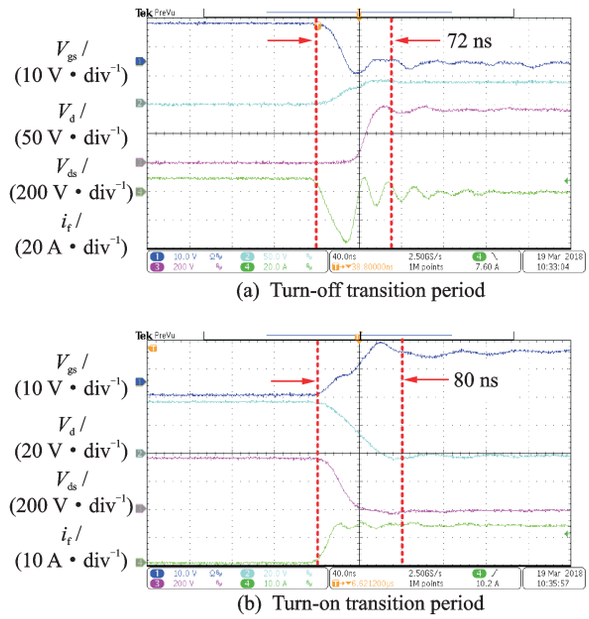
Fig.18 and Fig.19 show the double-pulse test transition waveforms of 150 V and 650 V ACDs, respectively. Fig.18(a) and Fig.19(a) are the turn-off transitions, while Fig.18(b) and Fig.19(b) are the turn-on transition. During the turn-off transition, when i_f drops to zero, V_d increases immediately as V_{gs} decreases. V_{ds} increases when V_{gs} decreases below the threshold value. During the turn-on transition, V_{ds} and V_d decrease in common with i_f increases and V_{gs} increases with V_d drops. When V_{gs} increases to the threshold value, V_{ds} drops to zero approximately. The 650 V ACD is more obvious, for high voltage MOSFET has smaller C_{ds} at high drain-source voltage. After some time delay V_d and V_{ds} drop to zero and V_{gs} reaches to the high value, then the MOSFET fully turns on. The whole turn-off and turn-on transition process are consistent with the analysis in Section III. The only difference is voltage and current have a ringing period at the end of the transition process. The ringing in forward current is a normal phenomenon at turn-off period. The reason of this ringing is that the parasitic inductor will resonant with the junction capacitor. For the consideration of efficiency, ACD needs to decrease the parasitic inductance.



(a) Turn-off transition period

(b) Turn-on transition period

Fig.18 Transition waveform of 150 V voltage specification ACD



(a) Turn-off transition period

(b) Turn-on transition period

Fig.19 Transition waveform of 650 V voltage specification ACD

3.2 Experimental results in LLC converter secondary-rectifier circuit with ACD

To evaluate the performance of proposed ACD in high operation frequency, a LLC resonant converter is developed in Fig.20.

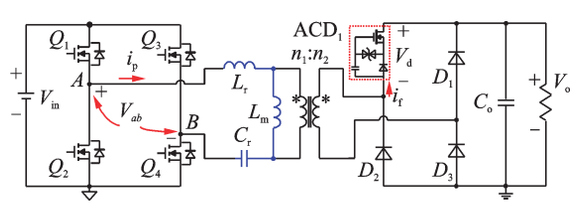


Fig.20 Topology of LLC converter with ACD

The primary inverter and secondary rectifier both use the full-bridge circuit. Table 1 shows the circuit parameters. In the prototype, the 650 V ACD is used to replace the secondary rectifier diode.

Table 1 Circuit parameters of experimental prototype

Parameter	Value
Input voltage V_{in} / V	400
Output voltage V_o / V	340
Max output power P_{omax} / W	1 400
Resonant capacitor C_r / nF	15
Resonant inductance L_r / μH	160
Magnetic inductance L_m /μH	640
Output capacitor C_o / μF	330
Power switch Q	IPB60R099C7
Rectifier diode D	DSEP-2906A
Resonant frequency f_r / kHz	100

Fig.21 gives the steady-state waveforms of LLC converter with ACD. It can be seen that ACD realizes the function of the diode. And some reverse recovery current is used to provide the driving energy.

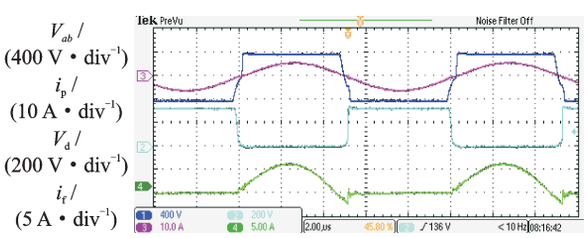


Fig.21 Steady-state waveforms of LLC converter with ACD

Fig.22 shows an efficiency comparison between the proposed 650 V ACD and the traditional 650 V fast recovery diode DSEP-2906A in the LLC converters with the same specifications. The efficiency of proposed ACD is 0.2% lower than traditional power diode DSEP-2906A in full load condition. The reason for this result is that ACD is built with discrete devices soldering on PCB. It introduces multiple parasitic inductances, which will definitely result in long time damping of voltage and current at switching transition process, leading to higher switching loss[18]. With two-die co-package structure, the performance should be much better than this discrete device structure. To verify this result, Fig.22 also gets the simulation result with co-package parasitic parameter ACD. It can be seen that with co-package, the efficiency benefit of ACD is obvious in full load range.

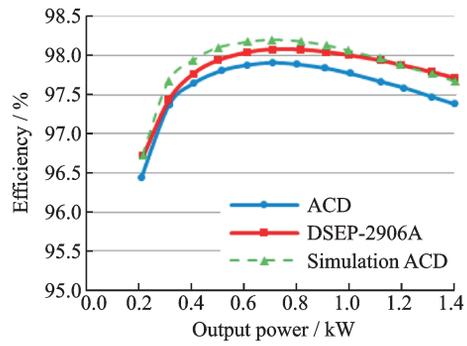


Fig.22 Efficiency comparison between ACD and the fast recovery diode in LLC converter

4 Conclusions

This paper proposes the ACD based on silicon MOSFET and Schottky diode, which can replace traditional power diode directly. The forward characteristic analysis has been conducted to show that the conduction loss of ACD is less than power diode. To evaluate the dynamic characteristic, switching behavior analysis is also given. Based on that, the double-pulse test is applied to verify the analytical characteristic and switching behavior. Finally, practical design with the proposed ACD in a LLC converter is finished in lab. The results show that the proposed ACD is practical, and it can realize high performance self-driven synchronous rectification with low cost. And if with a real co-package, the performance will be even better.

References

[1] TABISZ W A, LEE F C, CHEN D Y. A MOSFET resonant synchronous rectifier for high-frequency DC/DC converters[C]// IEEE Power Electronics Specialists Conference. [S.l.]: IEEE, 1990.

[2] KIM B S, RYU H S, SHIN M S, et al. Design of flyback converter with voltage driven synchronous rectifier[C]// Power Electronics and Motion Control, 2006, 12th International Conference on. [S. l.]: IEEE, 2006.

[3] GARCIA O. Zero voltage switching in the PWM half bridge topology with complementary control and synchronous rectification [C]// IEEE PESC'95. [S.l.]: IEEE, 1995.

[4] MA Y, XIE X G, QIAN Z. Frequency-controlled LCC resonant converter with synchronous rectifier

[C]// Power Electronics and Drive Systems, 2007, 7th International Conference on. [S.l.]: IEEE, 2007.

[5] JI H K, KIM H J. Active clamp forward converter with MOSFET synchronous rectification[C]// Power Electronics Specialists Conference, 25th Annual IEEE. [S.l.]: IEEE, 1994.

[6] JOVANOVIC M M, ZHANG M T, LEE F C. Evaluation of synchronous-rectification efficiency improvement limits in forward converters[J]. IEEE Transactions on Industrial Electronics, 1995, 42(4): 387-395.

[7] ZHANG M T, JOVANOVIC M M, LEE F C. Design considerations and performance evaluations of synchronous rectification in flyback converters [C]// Applied Power Electronics Conference and Exposition, 1997, 12th Annual. [S.l.]: IEEE, 1997.

[8] XIE X F, YAN C H, PONG M H. Studies of self-driven synchronous rectification in low voltage power conversion[C]// Power Electronics and Drive Systems, 1999, Proceedings of the IEEE 1999 International Conference on. [S.l.]: IEEE, 1999.

[9] ZHONG W X, HUI S Y, HO W C, et al. Using self-driven AC-DC synchronous rectifier as a direct replacement for traditional power diode rectifier [J]. IEEE Transactions on Industrial Electronics, 2012, 59(1): 392-401.

[10] XIE X F, LIU J C P, POON F N K, et al. A novel high frequency current-driven synchronous rectifier applicable to most switching topologies [J]. IEEE Transactions on Power Electronics, 2001, 16(5): 635-648.

[11] YUAN B, XU M, YANG X, et al. A new structure of LLC with primary current driven synchronous rectifier [C]// IEEE International Power Electronics & Motion Control Conference. [S.l.]: IEEE, 2009.

[12] SAKAI E, HARADA K. A new synchronous rectifier using bipolar transistor driven by current transformer [C]// IEEE Telecommun Energy Conference, INTELEC'92. [S.l.]: IEEE, 1992: 424-429.

[13] ACKER B, SULLIVAN C R, SANDERS S R. Current-controlled synchronous rectification [C]// IEEE Appl Power Electron Conference. [S. l.] : IEEE, 1994: 185-191.

[14] YEE H P, MEYER S, HORIGUCHI K, et al. A self-driven synchronous rectifier [C]// IEEE Power Electronics Specialists Conference. [S.l.]: IEEE, 1994: 627-633.

[15] LIN Congzhi, HE Mingxie, REN Xiaoyong, et al. 1 MHz GaN LLC resonant converter with matrix transformer[J]. Journal of Nanjing University of Aeronautics and Astronautics, 2018, 50(5): 695-700. (in Chinese)

[16] REN Xiaoyong, CHEN Yu, TONG Dan, et al. A nonlinear control strategy for Vienna rectifier under unbalanced input voltage [J]. Transactions of Nanjing University of Aeronautics and Astronautics, 2019, 36 (5): 703-714.

[17] VAZQUEZ A, RODRIGUEZ A, FERNANDEZ M, et al. On the use of front-end cascode rectifiers based on normally on SiC JFET and Si MOSFET [J]. IEEE Transactions on Power Electronics, 2014, 29(5): 2418-2427.

[18] HUANG X C, LIU Z Y, LEE F C, et al. Characterization and enhancement of high-voltage cascode GaN devices[J]. IEEE Transactions on Electron Devices, 2015, 62(2): 270-277.

Acknowledgement This work was supported in part by the National Natural Science Foundation of China (No. 51777093).

Authors Prof. **REN Xiaoyong** received the B. S., M. S. and Ph. D. degrees in Electrical Engineering from Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, P. R. China, in 2002, 2005 and 2008, respectively. His current research interests include DC-DC conversion, converter control techniques, GaN device application and renewable power systems.

Mr. **LI Kunqi** received his B.S. degree from NUAA in 2017. Now he is currently working toward the M.S. degree at the Aero-Power Sci-Tech Center, NUAA. His research interests include the high power density convert and power device.

Prof. **CHEN Qianhong** received the B.S. and Ph.D. degrees in electrical engineering from NUAA, Nanjing, China, in 1995, 1998 and 2001, respectively. She is currently a Professor with the Aero-Power Sci-Tech Center. Her research interests include application of integrated-magnetics, wireless power transfer.

Author contributions Prof. **REN Xiaoyong** contributed to the guide of the circuit design and model analysis. Mr. **LI Kunqi** contributed to complying the models, conducting the analysis, and writing the manuscript. Prof. **CHEN Qianhong** contributed to the guide of the magnets design and circuit control. All authors commented on the manuscript draft and approved the submission.

Competing interests The authors declare no competing interests.

(Production Editor: Zhang Huangqun)