An Improved Active Miller Clamp Crosstalk Suppression Method for Enhancement-Mode GaN HEMTs in Phase-Leg Configuration

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Abstract: When using traditional drive circuits, the enhancement-mode GaN (eGaN) HEMT will be affected by high switching speed characteristics and parasitic parameters leading to worse crosstalk problems. Currently, the existing crosstalk suppression drive circuits often have the disadvantages of increased switching loss, control complexity, and overall electromagnetic interference (EMI). Therefore, this paper combines the driving loop impedance control and the active Miller clamp method to propose an improved active Miller clamp drive circuit. First, the crosstalk mechanism is analyzed, and the crosstalk voltage model is established. Through the crosstalk voltage evaluation platform, the influencing factors are evaluated experimentally. Then, the operating principle of the improved active Miller clamp drive circuit is discussed, and the optimized parameter design method is given. Finally, the effect of the improved active Miller clamp method for suppressing crosstalk is experimentally verified. The crosstalk voltage was suppressed from 3.5 V and −3.5 V to 1 V and −1.3 V, respectively, by the improved circuit.

Key words: enhancement-mode GaN (eGaN); crosstalk suppression; gate driver; high-speed switching; active clamp

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0 Introduction

As one of wide bandgap semiconductor devices, the the enhancement-mode GaN (eGaN) HEMT has lower on-resistance, smaller junction capacitance, faster switching speed, and better high temperature resistance than Si devices.

The power electronic converter based on eGaN HEMT is expected to significantly increase the maximum working frequency and efficiency, and reduce its volume and weight[1-4]. Therefore, eGaN HEMT has very broad application prospects in aerospace, radio energy transmission, electric vehicles, new energy power generation and other fields[5]. In the aerospace field, the weight of power converter in the power system of distributed electric propulsion aircraft accounts for more than 30% of the total weight of the electrical system. The use of eGaN HEMT can play a great role in improving system efficiency, reducing the system power density and the cost of heat dissipation device[6-7].

When GaN devices are used in half-bridge topology such as buck converters and inverters, crosstalk is one of the most common and serious problems. Although shoot-through issue in a phase-leg configuration can be avoided as much as possible by adding dead time, high dv/dt of one switch will interact with the parasitic capacitance of its complementary switch, and Miller current will be injected towards Miller capacitance, thereby generating

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crosstalk voltage.

Among them, the positive crosstalk voltage may cause unexpected turn-on of the power transistor which should be turned off, leading to the shoot-through problem. Compared with Si devices, GaN devices have faster switching speed and lower gate threshold voltage, which is prone to mislead[8-9]. And the negative crosstalk voltage is likely to exceed the maximum gate-source negative voltage range, resulting in device damage, especially compared with Si devices, the allowable range of gate-source negative voltage of eGaN HEMT is smaller[10]. Thus, to fully take advantage of the high switching speed of GaN devices and guarantee reliability of the phase-leg configuration, crosstalk suppression methods need to be studied.

Prior reported work has proposed several methods for crosstalk mitigation. They can be divided into two categories.

(1) Apply the negative-biased turn-off gate voltage. During the off state, when the negative bias voltage is added to gate-source of switch, the positive crosstalk voltage is superimposed with the negative bias voltage, thus reducing the positive crosstalk voltage amplitude[11-13]. However, it aggravates the impact of negative crosstalk and is very likely to damage power devices. And for eGaN HEMT, this kind of method increases the reverse conduction loss and reduces the system efficiency. Ref.[14] used RC delay circuit as the control signal of auxiliary circuit to achieve the negative gate-source voltage during the positive crosstalk period to avoid false turn-on, and achieved zero gate-source voltage during negative crosstalk period to avoid the negative overvoltage breakdown. Meanwhile, the complexity of driving circuit was increased, and the selection of negative gate-source voltage was limited by the allowable range of gate-source negative voltage of eGaN HEMT[15].

(2) Control the gate drive impedanc. Ref.[16] connected an external capacitance in parallel between gate and source of switch to provide a low impedance branch for Miller current, which effectively suppressed crosstalk voltage. However, it increased the gate-source equivalent capacitance and reduced the switching speed of power device at the same time, thereby increased the switching loss[17]. In Ref.[18], a controllable capacitance was connected in parallel at the gate source stage of the device. When the device was in freewheeling state, the controllable capacitance worked, which was equivalent to increasing the gate-source capacitance, so as to suppress crosstalk. When it was used as an active switch, the controllable capacitance was disconnected to avoid increasing switching loss. The active Miller clamp suppression method was adopted in Refs.[19-20]. It reduced the influence of external parallel gate-source capacitance on the switching speed. During crosstalk period, the auxiliary switch turned on, and most of Miller current flowed through this low impedance loop, thereby reduced crosstalk voltage.

In summary, for eGaN HEMT, crosstalk is a serious problem that limits its high-frequency advantages, and proposing a reliable suppression method of crosstalk is very important to the design of half-bridge circuit. In this paper, crosstalk mechanism is analyzed first. Then, through the establishment of a crosstalk voltage evaluation platform, the impact factors of the crosstalk voltage are evaluated experimentally. Finally, the principle analysis and key parameter design guidelines of the improved crosstalk suppression method are given, and its effectiveness is verified by experimental results.

1 Principle and Modeling of Crosstalk

1.1 Principle of crosstalk

Fig.1 shows the schematic diagram for illustrating the occurrence of crosstalk voltage in a half bridge topology when Q_1 is turned on. In Fig.1, Q_2 and Q_1 are the high side switch and the low side switch, respectively. R_{G2} and R_{G1} are the total driving resistances, including the internal resistance of the driving chip, the external gate resistance and the internal resistance of eGaN HEMT. In actual driving circuit, the drive-on circuit and the drive-off circuit are usually independent of each other, so turn-

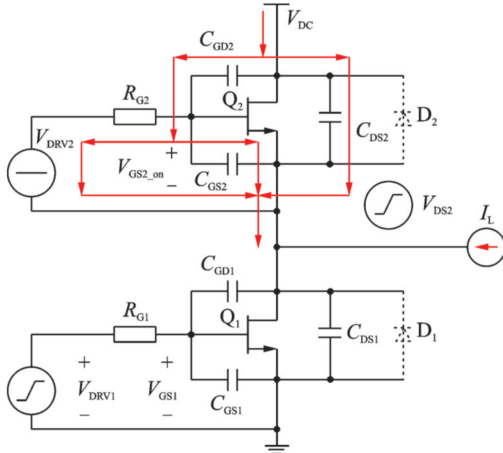


Fig.1 Schematic diagram for illustrating occurrence of crosstalk voltage in a half bridge topology when Q_1 is turned on

on gate resistance and turn-off gate resistance can be adjusted independently, and a total equivalent resistance is used instead. V_{DRV1} and V_{DRV2} are the turn-on gate voltages, C_{GD2}, C_{GS2}, C_{DS2}, C_{GD1}, C_{GS1} and C_{DS1} are the device junction capacitances. Due to the symmetric lateral structure between drain and source without P-N junctions, eGaN HEMT can be bi-directionally conducted in the channel. D_2 and D_1 are diode-like diodes of eGaN HEMT, which can characterize reverse conduction ability. V_{DC} is the power supply of DC-link and I_L is the equivalent current source. Here, Q_1 is the active switch. V_{GS1} is the gate-source voltage of Q_1, V_{GS2_on} is the positive crosstalk voltage of Q_2 and V_{DS2} is the drain-source voltage of Q_2.

The waveform representing the gate-source voltage behaviour is shown in Fig.2. Before Q_1 is turned on, the bridge-arm circuit is in the dead time period and the driving signals are low level. At this time, I_L continues to flow through Q_2.

During the turn-on process of Q_1, that is, V_{GS1} rises from the threshold voltage $V_{GS(TH)}$ to the Miller platform voltage V_p, Miller current is injected towards the gate by the Miller capacitance of complementary high side switch Q_2, thereby generating a positive voltage spike V_{GS2_on}. If the voltage spike exceeds the gate-source threshold voltage of eGaN HEMT, the high side switch will suffer from induced turn-on, which in turn causes a shoot-through across the half bridge.

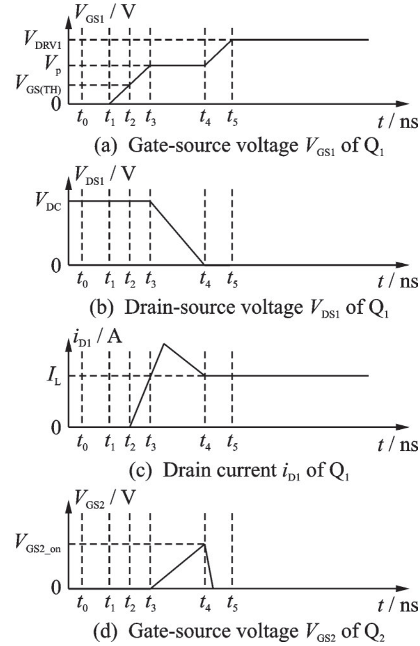


Fig.2 Waveform representing gate-source voltage behaviour when Q_1 is turned on

Fig.3 shows schematic diagram for illustrating the occurrence of crosstalk voltage when Q_1 is turned off. During the turn-off process of Q_1, Miller current is injected towards the Miller capacitance of complementary high side switch Q_2, thereby generating a negative voltage spike V_{GS2_off}. If the voltage spike exceeds the maximum negative voltage that gate-source of eGaN HEMT can withstand, the switch will be damaged. The waveform representing the gate-source voltage behaviour is shown in Fig.4.

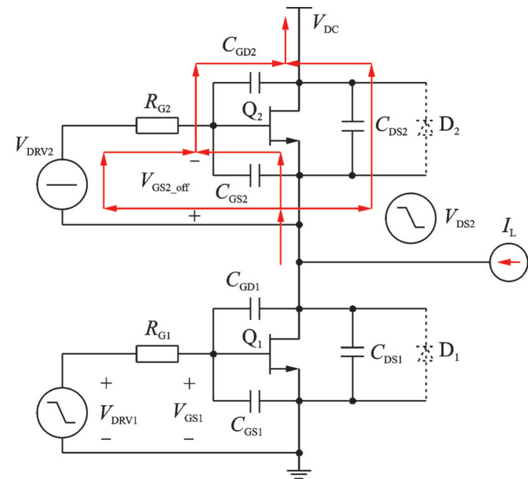


Fig.3 Schematic diagram for illustrating occurrence of crosstalk voltage in a half bridge topology when Q_1 is turned off

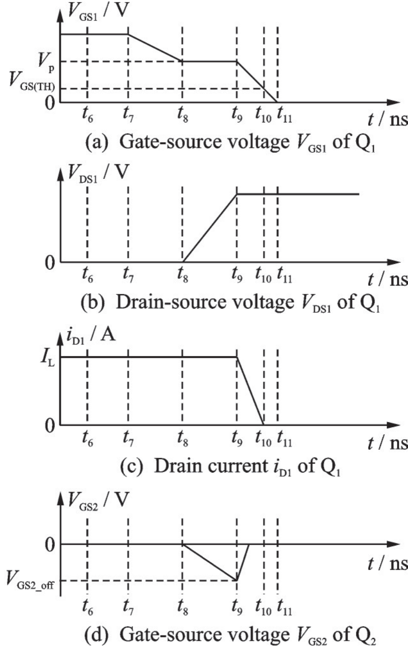


Fig.4 Waveforms representing gate-source voltage behaviour when Q_1 is turned off

1.2 Modeling of crosstalk

The equivalent circuit representing the positive crosstalk behavior during Q_1 turning on transient is shown in Fig.5, where V_{DS2} is the drain-source voltage of Q_2, R_{G2_off} the turn-off gate resistance of Q_2, i_{DG2} the current flowing in C_{GD2}, i_{GS2} the current flowing in C_{GS2}, and i_{G2} the current flowing in R_{G2_off}.

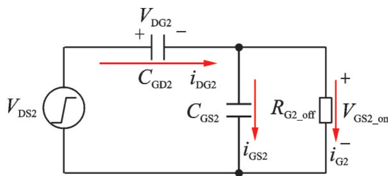


Fig.5 Equivalent circuit representing positive crosstalk behavior during Q_1 turning on transient

According to Kirchhoff's voltage law (KVL) and Kirchhoff's current law (KCL), Eq.(1) can be obtained from Fig.5.

$$-C_{GD2}\frac{dV_{DS1}}{dt}=(C_{GS2}+C_{GD2})\frac{dV_{GS2_on}}{dt}+\frac{V_{GS2_on}}{R_{G2_off}} \tag{1}$$

where C_{GD2} is the Miller capacitance of Q_2, V_{DS1} the drain-source voltage of Q_1, C_{GS2} the gate-source capacitance of Q_2, R_{G2_off} the turn-off gate resistance of Q_2, and V_{GS2_on} the positive crosstalk voltage.

V_{GS2_on} can be expressed as

$$V_{GS2_on}=-R_{G2_off}\cdot C_{GD2}\cdot\frac{dV_{DS1}}{dt}\cdot\left(1-e^{\frac{-t}{R_{G2_off}(C_{GD2}+C_{GS2})}}\right) \tag{2}$$

where V_{DC} is the bus voltage and V_{DS2} the drain-source voltage of Q_2. When V_{DS1} drops to zero, V_{GS2_on} reaches the maximum $V_{GS2_on(max)}$

$$V_{GS2_on(max)}=R_{G2_off}\cdot C_{GD2}\cdot\frac{V_{DC}}{T_{DS1}}\cdot\left(1-e^{\frac{-T_{DS1}}{R_{G2_off}(C_{GD2}+C_{GS2})}}\right) \tag{3}$$

where T_{DS1} is the time when V_{DS1} drops from V_{DC} to zero.

It can be seen from Eq.(3) that the influencing factors of $V_{GS2_on(max)}$ include R_{G2_off}, C_{GS2} and T_{DS1}, which also have impact on the switching-on speed of Q_1.

Similarly, when V_{DS1} rises to V_{DC}, the negative crosstalk voltage spike $V_{GS2_off(max)}$ is

$$\left|V_{GS2_off(max)}\right|=R_{G2_off}\cdot C_{GD2}\cdot\frac{V_{DC}}{T_{DS2}}\cdot\left(1-e^{\frac{-T_{DS2}}{R_{G2_off}\cdot C_{GS2}}}\right) \tag{4}$$

It can be seen from Eq.(4) that the influencing factors of $V_{GS2_off(max)}$ include R_{G2_off}, C_{GS2} and T_{DS2}, which also have impact on the switching-off speed of Q_1.

2 Evaluation Results of Impact Factors

As shown in Fig.6, the evaluation of factors affecting crosstalk is conducted by a double pulse experiment platform (DPT). The power device adopts GS66506T (650 V/22.5 A) of GaN systems. During the experiment, by short-circuiting gate-source of top switch, the crosstalk effect on the gate-source of top switch caused by switching action of bottom switch is investigated.

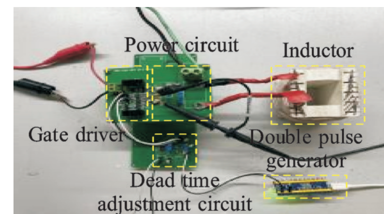


Fig.6 Experimental setup of DPT

2.1 Impact of load current and bus voltage

When the bus voltage is 400 V, the crosstalk

voltage is evaluated when the load current i_D is 2, 4, 6 and 8 A. The typical waveforms are shown in Fig.7. Fig.8 shows the relationship curves of crosstalk voltage of top switch with the change of load current.

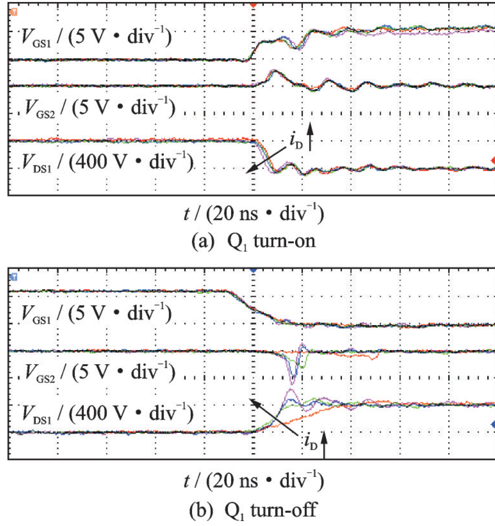


Fig.7 Crosstalk voltage waveforms of top switch under different load currents

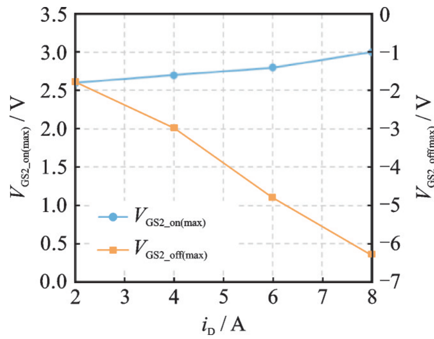


Fig.8 Relationship curves between crosstalk voltage of top switch and load current

During the turn-on process of Q_1, the slew rate of drain-source voltage only slightly increases with the rise of load current, and the crosstalk voltage of Q_2 increases from 2.6 V to 3 V without significant change. During the turn-off process, the switching speed of Q_1 increases due to the increasing of load current. Therefore, the slew rate of drain-source voltage increases significantly, resulting in a negative crosstalk voltage decreasing from −1.8 V to −6.3 V. Meanwhile, the time when the negative crosstalk voltage reaches the lowest point is also advanced accordingly.

When load current is 4 A, the crosstalk voltage is evaluated when the bus voltage V_{DC} is 100, 200, 300 and 400 V. The typical waveforms are shown in Fig.9, and Fig.10 shows the relationship curves of crosstalk voltage of top switch with the change of bus voltage.

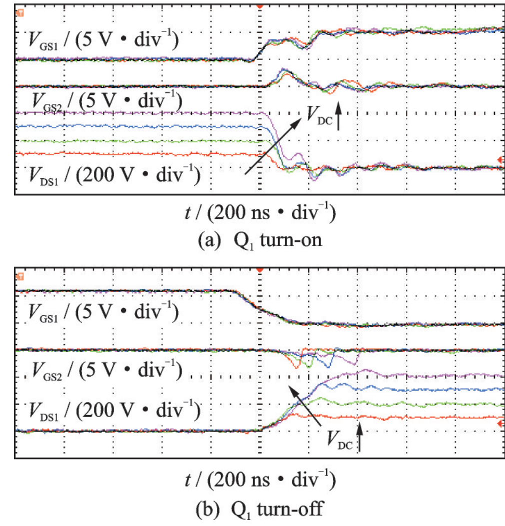


Fig.9 Crosstalk voltage waveforms of top switch under different bus voltages

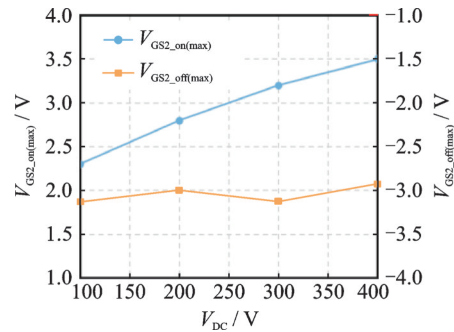


Fig.10 Relationship curves between crosstalk voltage of top switch and bus voltage

During the turn-on process of Q_1, as bus voltage increases, the slew rate of drain-source voltage increases significantly, which causes the positive crosstalk voltage increase from 2.3 V to 3.5 V. During the turn-off process, the rise rate of drain-source voltage is basically unchanged, so the negative crosstalk voltage of Q_2 remains at −3 V. At the same time, the time point when the negative crosstalk voltage reaches the lowest point is also delayed accordingly.

2.2 Impact of gate-source external capacitance

When the load current is 6 A and the bus volt-

age is 400 V, the crosstalk voltage is evaluated when the gate-source external capacitance $C_{GS_external}$ is 0, 0.2, 0.4, 0.6, 0.8, 1.0 nF. The typical waveforms are shown in Fig.11 and the relationship curves between the crosstalk voltage and the gate-source external capacitance are shown in Fig.12.

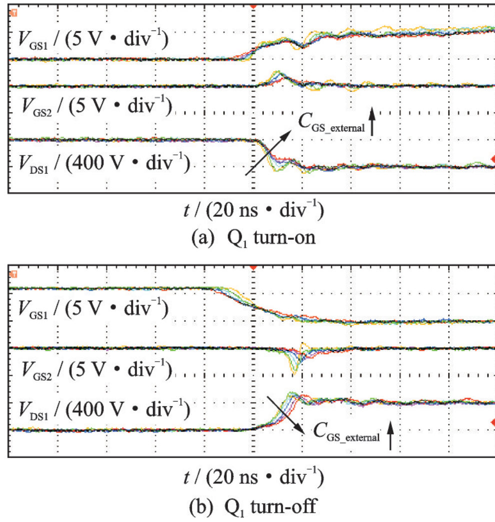


Fig.11 Crosstalk voltage waveforms of top switch under different gate-source external capacitances

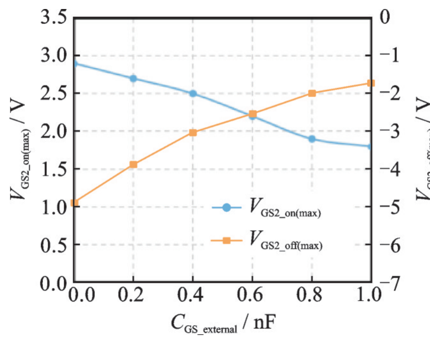


Fig.12 Relationship curves between crosstalk voltage of top switch and gate-source external capacitance

During the turn-on process of Q_1, as the external gate-source capacitance increases, the gate-source voltage rises slower and the oscillation slows down. At the same time, the drain-source voltage drop rate decreases and the positive crosstalk voltage of Q_2 decreases correspondingly. Under the dual influence of the drain-source voltage change rate and the gate-source capacitance itself, when the gate-source external capacitance increases from 0 nF to 1 nF, the positive crosstalk voltage decreases from 2.9 V to 1.8 V. In the same way, during turn-off process of Q_1, with the increase of external capacitance, the absolute value of negative crosstalk voltage decreases significantly, from −4.9 V to −1.8 V.

Although the increasing gate-source external capacitance has a significant suppression effect on the crosstalk voltage, it is not suitable to be adopted at the expense of significantly increasing the turn-on, turn-off and total losses of bottom switch (E_{on}, E_{off}, E_{total}) and sacrificing the performance advantages of high switching speed and low switching loss, as shown in Fig.13.

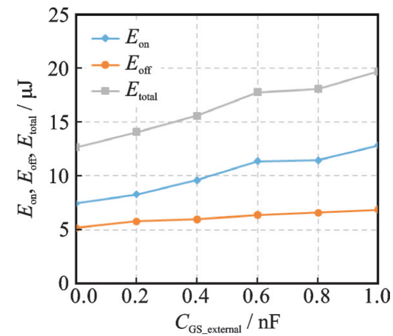
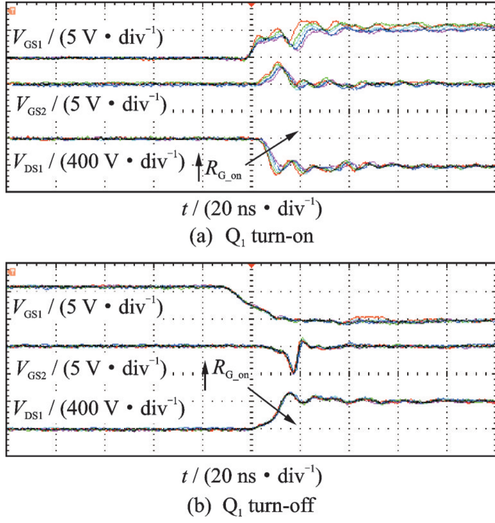


Fig.13 Relationship curves between turn-on, turn-off and total losses of Q_1 and gate-source external capacitance

2.3 Impact of turn-on gate resistance

When the load current is 6 A and the bus voltage is 400 V, the crosstalk voltage waveform under different turn-on gate resistance R_{G_on} are shown in Fig.14. Fig.15 shows the relationship curves of crosstalk voltage of top switch with the change of turn-on drive resistance.

It can be seen that during the turn-on process of Q_1, as the turn-on drive resistance increases, the rate of gate-source voltage slows down and the oscillation decreases. Due to the increase of turn-on drive resistance, the discharge speed of gate-drain capacitance slows down, which results in a slower rate of drain-source voltage rise, and further reduces the positive crosstalk voltage of Q_2. The turn-on gate resistance itself has no effect on crosstalk voltage, and it mainly affects the crosstalk voltage indirectly by changing the rate of drain-source voltage. During the turn-off process of Q_1, since the change of turn-on drive resistance has no effect on dv/dt, the negative crosstalk voltage remains unchanged.



(a) Q_1 turn-on

(b) Q_1 turn-off

Fig.14 Crosstalk voltage waveforms of top switch under different turn-on gate resistances

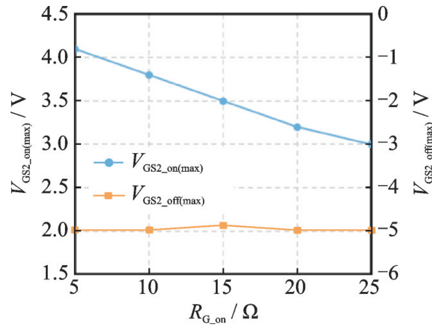


Fig.15 Relationship curves between crosstalk voltage of top switch and turn-on gate resistance

From the above analysis, although the increasing turn-on gate resistance has a significant suppression effect on the crosstalk voltage, it is not suitable to be adopted because it will reduce the switching speed and increase the switching loss, as shown in Fig.16. When the turn-on drive resistance increases from 5 Ω to 25 Ω, the total switching loss E_{total} of bottom switch increases from 7.798 μJ to 13.331 μJ, increased by 71%.

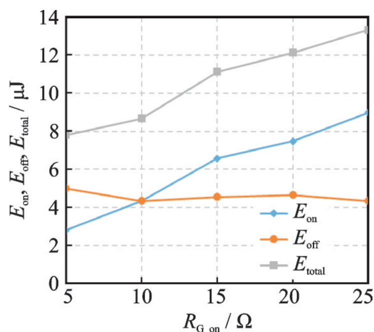


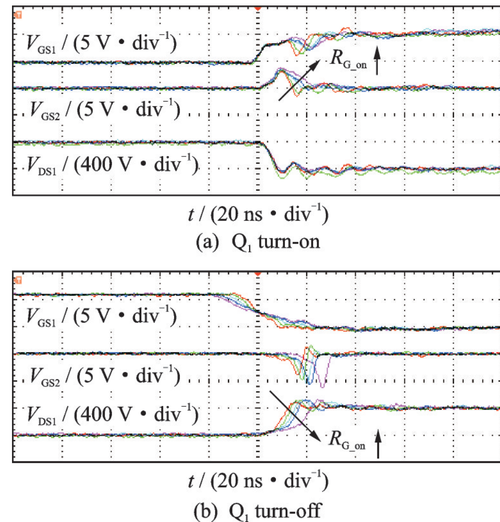
Fig.16 Relationship curves between turn-on, turn-off and total losses of Q_1 and turn-on gate resistance

2.4 Impact of turn-off gate resistance

On one hand, the turn-off drive resistance R_{G_off} indirectly affects crosstalk voltage by affecting the rate of drain-source voltage during the turn-off process. On the other hand, it will directly affect the crosstalk voltage to a certain extent because the turn-off drive resistance is in the gate turn-off loop.

As shown in Fig.17 and Fig.18, during the turn-on process of Q_1, as the turn-off gate resistance increases from 5 Ω to 25 Ω, the positive crosstalk voltage increases from 2.9 V to 3.7 V. Since the turn-off drive resistance basically has no influence on dv/dt of drain-source voltage during the turn-on process, the effect of turn-off gate resistance on the positive crosstalk voltage is mainly due to the impact of drive turn-off loop impedance. During the turn-off process of Q_1, under the combined action of two influencing factors, the influence of turn-off driving resistance itself is more significant, so the final result is that the absolute value of negative crosstalk voltage of Q_2 increases with the increasing turn-off gate resistance. When the turn-off drive resistance increases from 5 Ω to 25 Ω, the negative crosstalk voltage changes from −3.7 V to −6.3 V.

Fig.19 illustrates the relationship curves between turn-on, turn-off and total losses (E_{on}, E_{off}, E_{total}) of bottom switch and turn-off gate resistance. Reducing the turn-off gate resistance has obvious effects on suppressing the crosstalk voltage and reduc-



(a) Q_1 turn-on

(b) Q_1 turn-off

Fig.17 Crosstalk voltage waveforms of top switch under different turn-off gate resistances

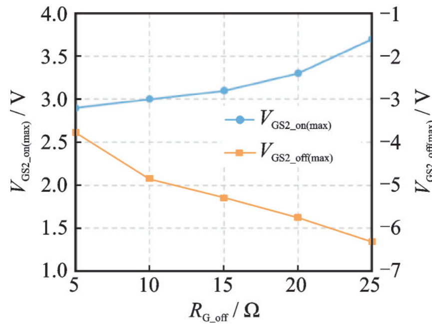


Fig.18 Relationship curves between crosstalk voltage of top switch and turn-off gate resistance

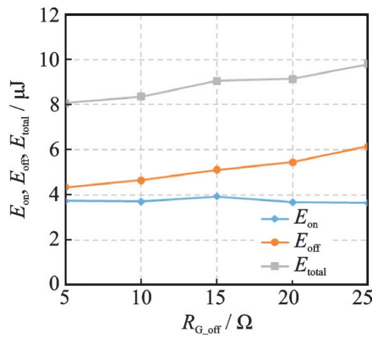


Fig.19 Relationship curves between bottom turn-on, turn-off and total losses of Q_1 and turn-off gate resistance

ing the loss, but simultaneously it will cause a significant increase in the drain-source voltage spike when the power device is turned off.

Through the evaluation of impact factors, it shows that the increasing gate-source external capacitance has a significant suppression effect on positive and negative crosstalk voltages, however, it is not suitable to be adopted directly because it will reduce the switching speed and increase the switching loss. The increasing turn-on gate resistance can also effectively reduce the positive crosstalk voltage at the expense of switching speed. Reducing the turn-off gate resistance has obvious effects on suppressing negative crosstalk voltage and reducing loss, but simultaneously it will cause a significant increase in the drain-source voltage spike when the power device is turned off. Thus, only adjusting the gate-source external capacitance, turning on the gate resistance or turning off the gate resistance cannot appropriately suppress crosstalk voltage, because it will bring about the increased switching loss or the increased voltage spikes. Therefore, it is necessary to seek effective suppression method.

3 Improved Active Suppression Method

The improved active Miller clamp circuit shown in Fig.20 provides an auxiliary branch for the flow of Miller current by connecting auxiliary switches Q_{aux1}, Q_{aux2} and auxiliary capacitances C_{aux1} and C_{aux2} in parallel at the gate and the source. G represents the gate of the switch, D the drain of the switch and S the source of the switch.

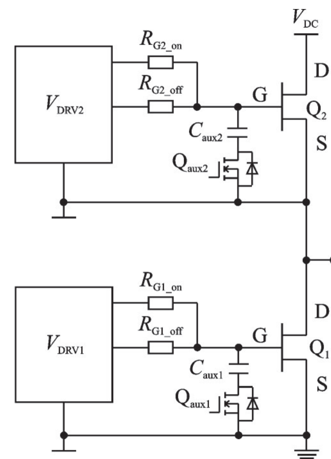


Fig.20 Active Miller clamp circuit

Fig.21 illustrates the switching timing diagrams of the improved active Miller clamp circuit. u_{Q2}, u_{Q1}, u_{aux1}, u_{aux2} are the driving voltages of Q_2, Q_1, Q_{aux1}, Q_{aux2}, respectively. After the auxiliary switch is turned on, the corresponding auxiliary capacitance is equivalent to increasing the gate-source capacitance of power switch, so as to suppress the crosstalk voltage. According to this switching sequence, since the auxiliary capacitor only works during the crosstalk period, it will not affect the switch-

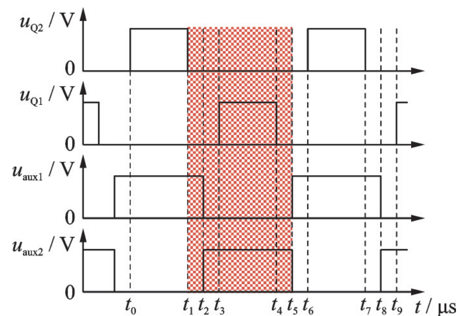


Fig.21 Switching sequence diagrams of active Miller clamp circuit

ing characteristics of the corresponding power switch.

Fig.22 shows the relationship curves between the crosstalk voltage and the auxiliary capacitance. It can be seen that with the increase of the auxiliary capacitance, the induced crosstalk voltage first decreases relatively in a slower rate, then decreases quickly, and at last decreases slowly too. Through trade-off, we finally choose the auxiliary capacitance value of 1 μF.

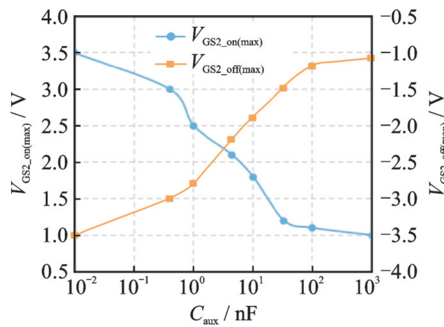


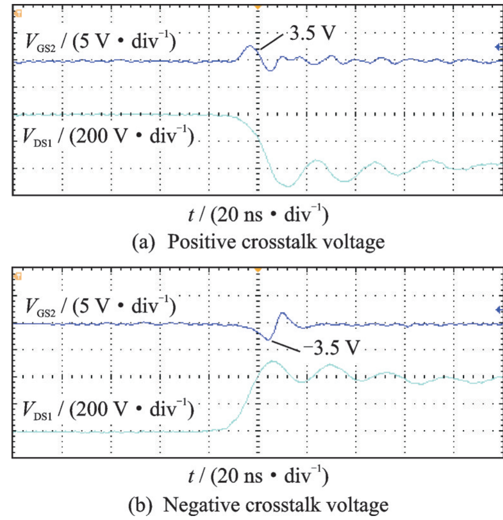
Fig.22 Relationship curves between crosstalk voltage and auxiliary capacitance

Table 1 shows the total loss of auxiliary switch Q_{aux2} and power switch Q_2 in a single switching cycle when C_{aux2}=1 μF. As can be seen from Table 1, the loss of crosstalk suppression circuit is very small, and the impact on the system is negligible.

Table 1 Q_{aux2} total loss and Q_2 total loss

C_{aux2} / μF	Total loss / μJ	
	Q_{aux2}	Q_2
1	0.025	97.975

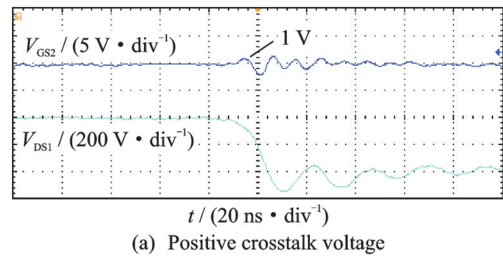
Figs. 23 and 24 illustrate the crosstalk voltage waveforms before and after crosstalk suppression circuit being used when the bus voltage is 400 V and the load current is 8 A, respectively. When the crosstalk suppression measure is not adopted, the positive and negative crosstalk voltages are 3.5 V and −3.5 V, respectively. The positive and negative crosstalk voltages are reduced to 1 V and −1.3 V, respectively, after using the active Miller clamp circuit, and the suppression effect is obvious, which can meet the crosstalk suppression requirement of eGaN HEMT.



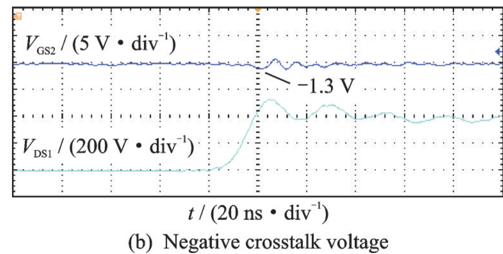
(a) Positive crosstalk voltage

(b) Negative crosstalk voltage

Fig.23 Positive and negative crosstalk voltage waveforms without crosstalk suppression



(a) Positive crosstalk voltage



(b) Negative crosstalk voltage

Fig.24 Positive and negative crosstalk voltage waveform when auxiliary capacitance is 1 μF

4 Conclusions

Based on the analytical and experimental investigations presented in this paper, the following conclusions can be drawn:

(1) Although the increasing gate-source external capacitance or the turn-on gate resistance has a significant suppression effect on the crosstalk voltage, it is not suitable to be adopted directly because it will reduce the switching speed and increase the switching loss. Reducing the turn-off gate resistance has obvious effects on suppressing the crosstalk voltage and reducing the loss, but simultaneously it will cause a significant increase in the drain-source voltage spike when the power device is turned off.

(2) Combining the turn-off loop impedance control with the active Miller clamp, an improved active Miller clamp crosstalk suppression method is realized. It effectively reduces the gate-source equivalent impedance during the crosstalk voltage generation stage, and does not affect the turn-on and the turn-off states of the power device.

(3) By optimizing the value of the auxiliary capacitance in the improved active Miller clamp branch, the crosstalk suppression effect can be enhanced.

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基于增强型GaN HEMT的改进型桥臂串扰抑制方法研究

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摘要:采用传统驱动电路时,增强型氮化镓(Enhancement-mode GaN,eGaN)HEMT会受高开关速度特性和寄生参数的影响,其桥臂串扰问题不容忽视,而已有桥臂串扰抑制驱动电路一般具有增加开关损耗、控制复杂程度和整机电磁干扰(Electromagnetic interference,EMI)的缺陷。为改进以上问题,本文结合驱动回路阻抗控制和有源密勒箝位方法,提出一种改进型有源密勒箝位驱动电路。首先分析了eGaN HEMT桥臂串扰的产生过程,建立了串扰电压模型,并通过桥臂串扰电压评估平台对各影响因素进行了实验评估。接着,研究了改进型有源密勒箝位驱动电路的工作原理,并通过实验对电容参数进行了优化选择。最后,对改进型有源密勒箝位方法抑制桥臂串扰的效果进行了实验验证,其将串扰电压分别从3.5 V和−3.5 V抑制到了1 V和−1.3 V。

关键词:增强型氮化镓;串扰抑制;栅极驱动;高速开关;有源钳位