

# A Current Mode Low-Noise Gm-C Filter with a Cut-Off Frequency of 5 GHz in Telecommunication System

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**Abstract:** The high linearity low-noise filter is an indispensable key circuit in the communication system. Based on the structure of current-reuse source-degradation operational transconductance amplifier (OTA), a 5 GHz current-mode low-noise Gm-C filter suitable for high-speed communication systems is proposed. Thanks to the proposed current mode structure and the OTA's high-power efficiency and high linearity, the filter obtains good noise and high linearity performance with very low power consumption. The filter is designed in standard 65 nm CMOS technology and occupies a core area of 0.06 mm<sup>2</sup>. The simulation results show that the operating bandwidth is 5 GHz, the IIP3 is 35 dBm, and the power consumption is only 3.2 mW.

**Key words:** Gm-C filter; lowpass filter; current mode filter

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## 0 Introduction

Modern wireless telecommunication systems evolve towards broadband features with high filtering requirements for in-band and out-band blockers. Normally, out-band blockers are filtered out by off-chip surface acoustic wave (SAW) filters. The in-band blockers need to be filtered by an integrated filter when the RF signal is down converted to the baseband<sup>[1]</sup>. In direct conversion receivers with very wide baseband, the baseband signal is directly filtered and processed without the second down-conversion<sup>[2]</sup>. Typically, the frequency of this signal can be up to several Giga hertz. An on-chip filter with high speed and good performance is needed to process a small power signal among many interferers. Both high SNR and high IIP3 are required for the filter in this application scenario. To meet such requirements, a new current mode Gm-C filter structure is proposed in this paper, achieving low noise and high linearity performance based on a cur-

rent reused source degeneration operational transconductance amplifier (OTA).

This paper is organized as follows. Section 1 explains the traditional voltage mode Gm-C filter. Section 2 presents and explains the design details of the proposed current mode Gm-C filter. Then, a comparison analysis between the proposed filter and the traditional filter is undertaken in Section 3. Besides, the simulated results and the performance comparison with other state-of-the-art results are also presented. Finally, a summary is concluded.

## 1 Traditional Voltage Mode Gm-C Biquad

In a typical direct conversion receiver's structure, a filter can be inserted after the down mixer to filter out the unwanted signals. It is widely accepted that Gm-C filters are the best choices for high-speed systems<sup>[3-12]</sup>. Fig.1 shows a traditional voltage mode Gm-C biquad, which consists of at least four

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OTAs<sup>[13]</sup>. As shown in Fig.1, the first OTA, which is also called Gm1, is used to convert the input voltage signal to a current signal. The second OTA, called Gm2, is utilized to realize low resistance by connecting its input and output. The transfer function of the traditional Gm-C biquad is expressed as follows

$$H(s) = \frac{\frac{g_{m1}g_{m3}}{C_1C_2}}{s^2 + s\frac{g_{m2}}{C_1} + \frac{g_{m3}g_{m4}}{C_1C_2}} = \frac{\frac{g_m^2}{C_1C_2}}{s^2 + s\frac{g_m}{C_1} + \frac{g_m^2}{C_1C_2}} \quad (1)$$

where  $g_{m1,2,3,4} = g_m$ .

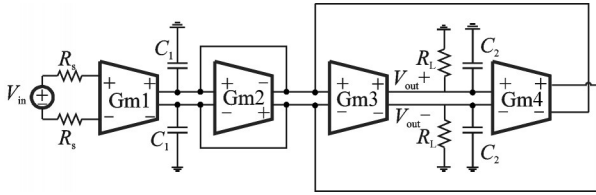


Fig.1 A traditional Gm-C biquad

For analysis convenience, the Gm-C biquad can be simplified in Fig.2. As discussed before, Gm1 cell generates a current signal from a voltage signal. With the help of capacitor  $C_1$ , Gm2 cell defines the first pole. Gm3, Gm4 and the output capacitor  $C_2$  compose a gyrator, which can be considered as an inductor  $L = C_2/g_{m3}g_{m4}$ . Consequently, Gm2 cell,  $C_1$  and  $L$  generate two poles. As a result, a second order lowpass filter is realized.  $\overline{dv_{eq}^2}$  is the equivalent input noise of the filter. With simulations and calculations, it is found that this voltage mode filter has a high noise figure (NF) and limited linearity. Among its components, Gm1 generates very large part of the noise and the none linearity.

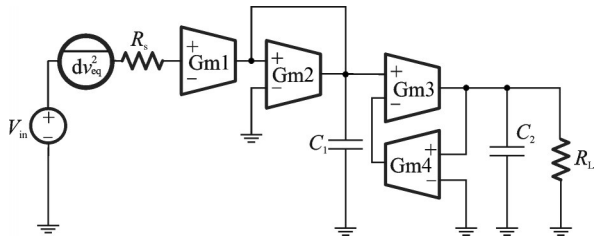


Fig.2 Simplified model of the traditional Gm-C biquad

## 2 A Current Mode Gm-C Biquad

To reduce noise and improve the linearity of a

Gm-C filter, several current mode filters were proposed<sup>[14-19]</sup>. Among them, Ref.[16] introduced a high linearity current mode noise shaping filter. But its bandwidth was only 2.8 MHz, which is not feasible for the wideband applications. The filter presented in Ref.[19] had a bandwidth of 1 GHz but a limited IIP3. To solve above issues, a high speed, low noise and high linearity current mode Gm-C biquad is proposed in this paper, as shown in Fig.3.

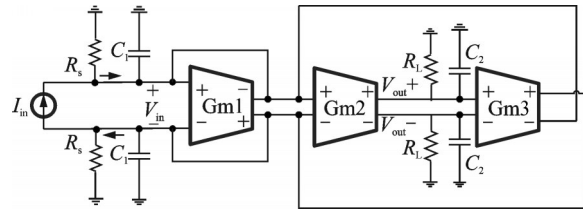


Fig.3 The proposed current mode biquad

The proposed biquad makes use of a high linearity complementary OTA shown in Fig.4 as its unit Gm cell. In the OTA structure, both NMOS pair and PMOS pair have been utilized for the input transistors, employing the same bias current. The current reuse technique has greatly increased the power efficiency of the circuit. The transistors  $M_P$  and  $M_N$  are added to act as the source degeneration resistors, improving the linearity of the OTA with an ability of transconductance adjustment. Besides,  $M_N$  is made by two identical transistors with the middle node  $V_N$  using for the common mode voltage in the common-mode feedback (CMFB) circuit. In this way, extra sensing resistors, are not needed for the common mode voltage. Moreover, since the OTA's common-mode output voltage is susceptible

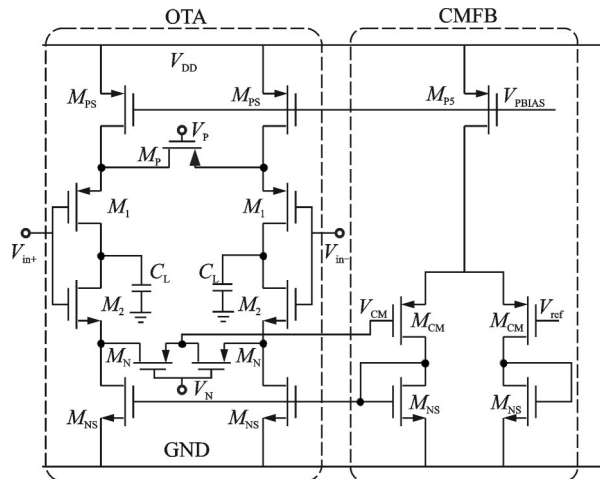


Fig.4 OTA structure including a CMFB

to the common-mode input signal disturbances and current source mismatches, the CMFB circuit shown in the right part of Fig.4 is utilized to stabilize it.

As shown in Fig.3, the proposed current mode biquad consists of three OTAs, four capacitors and two  $R_L$ . The structure gets rid of the first voltage to current transformation OTA in the traditional Gm-C filter. In this way, the nonlinearity components coming from the first OTA in Fig.1 can be reduced. Besides, the input interferers can be filtered with the help of input capacitor  $C_1$  before they enter the nonlinear device. As a result, the proposed filter can achieve a very good IIP3 performance.

The transfer function of the proposed biquad is given by

$$\frac{V_{out}}{I_{in}} = \frac{g_m}{C_1 C_2} \frac{1}{s^2 + s \frac{g_m}{C_1} + \frac{g_m^2}{C_1 C_2}} \quad (2)$$

where  $g_{m1,2,3} = g_m$ .

Clearly, a second order low-pass function can still be realized by the structure, except that its input signal is in current domain. With calculation, the cut-off frequency of the current mode biquad is

$$\omega_0 = \pm g_m / \sqrt{C_1 C_2} \quad (3)$$

and the quality factor is

$$Q = \sqrt{C_1 / C_2} \quad (4)$$

where  $\omega_0$  is decided by the values of  $g_m$  and the capacitors  $C_1$  and  $C_2$ . Since large sizes of  $M_1$  and  $M_2$  generate large  $g_m$  but also large parasitic capacitance, an optimized value of  $g_m$  is chosen to be 1.7 ms in order to achieve a bandwidth of 5 GHz. Meanwhile,  $C_1$  and  $C_2$  are designed as 60 fF and 200 fF, leaving a certain margin for the layout of parasitic capacitance. Since the direct current (DC) gain of the OTA should be larger than 30 dB in a low  $Q$  filter<sup>[4]</sup>, the OTA gain is set to be 35 dB in this paper. Normally, the CMFB circuit needs sense resistors  $R$  to provide the common mode voltage. However, large sense resistors not only occupy large layout area, but also increase parasitic capacitance and degrade the OTA speed performance. As explained before, because of using the middle node

of the active resistance  $M_N$ , the large sense resistor  $R$  can be avoided in the design.

### 3 Comparison of Simulation Results Between the Proposed Current Mode Gm-C Biquad and the Traditional Gm-C Biquad

In order to compare the noise performances of the traditional voltage mode and the proposed current mode filters, source resistors are added at the inputs of the two Gm-C biquads to represent the output impedance of their previous stage, as shown in Fig.2 and Fig.5. In this way, these two filters have the same representations for their source resistances. As described in Section 2, the input equivalent noise of the voltage mode filter is represented by  $\overline{dv_{eq}^2}$ . In contrast, the current mode filter is actually driven by a current source, its input equivalent noise is represented by  $\overline{di_{eq}^2}$  and  $\overline{dv_{eq}^2}$ . Then the calculation of the two filters' NF can be simplified as Eqs.(5,6)<sup>[20]</sup>.

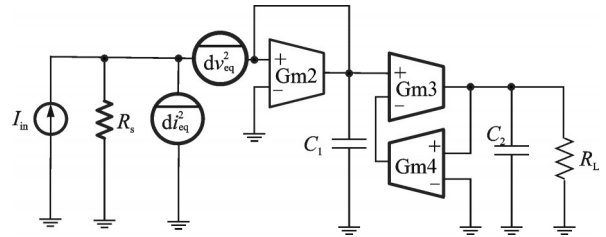


Fig.5 Noise model of current mode biquad including source resistors

$$NF_{\text{voltage mode}} = 10 \lg \left( 1 + \frac{\overline{dv_{eq}^2}}{4kTR_s df} \right) \quad (5)$$

$$NF_{\text{current mode}} = 10 \lg \left( 1 + \frac{\overline{dv_{eq}^2} + R_s^2 \cdot \overline{di_{eq}^2}}{4kTR_s df} \right) \quad (6)$$

where  $k$  is the Boltzmann's constant,  $T$  the absolute temperature, and  $f$  the frequency. Apparently, the NF of the voltage mode Gm-C filter is reverse proportional to its source resistance  $R_s$ . As a result, it will decrease when  $R_s$  increases. Differently, the NF of the current mode Gm-C filter has an optimum value when  $R_s$  is small. Consequently, the filter with a low source resistance should choose the current mode structure to improve its noise performance. Besides, from Eqs.(5, 6), it can be seen that the NF is

not influenced by the gain of two filters, meaning that the load impedance  $R_L$  will not affect their NFs.

For a fair performance comparison, the same OTA with a fixed  $g_m$  value for high-speed applications, shown in Fig.4, is used in the traditional voltage mode and the proposed current mode filters with their source impedance  $R_s$  setting to  $150 \Omega$ . The DC voltage gain of the filters is defined as  $A_{DC} = V_{out}/V_{in}$ , which is also influenced by  $R_L$ . Both filters have been designed with the same  $A_{DC}$  by using of suitable  $R_L$ , which will not affect the noise performance as explained before. Fig.6 shows the simulated transfer functions of the proposed current mode and traditional voltage mode filters. Clearly, these two filters have very similar lowpass transfer functions. As indicated, both filters have an DC gain of around 2.5 dB with a similar bandwidth of 5 GHz. Fig.7 shows the NF performances of the filters. Obviously, in the frequency range from DC to 5 GHz, the NF of the proposed current mode structure is about 5 dB less than that of the traditional structure. In a wideband communication system, a high-speed filter is always needed after a down mixer in a receiver

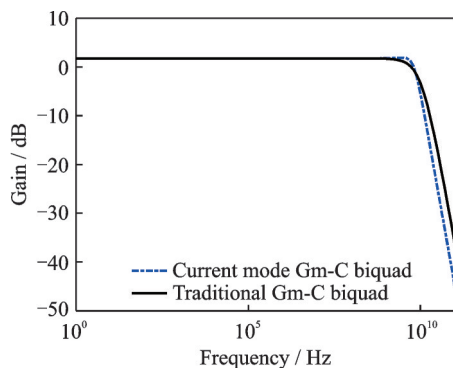


Fig.6 Simulated transfer functions of the traditional Gm-C biquad and the proposed current mode Gm-C biquad

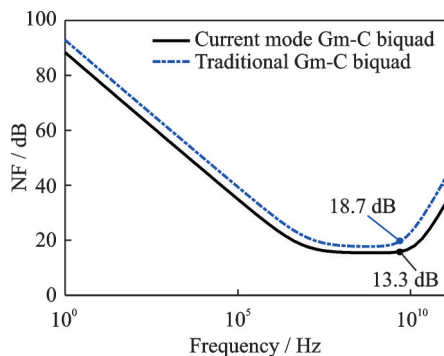


Fig.7 NF of two biquads

or after a high-speed digital to analog converter (DAC) in a transmitter. In both cases, the previous stage of the lowpass filter has a relatively low output impedance ranging from  $50 \Omega$  to  $300 \Omega$ <sup>[21-22]</sup>. Therefore, a current mode filter is preferable compared with the traditional structure in these scenarios.

Fig.8 shows the simulated IIP3 of the two structures with a 2 GHz and 2.1 GHz two-tone test. Clearly, the proposed current mode biquad has an IIP3 value of 35 dBm, which is 6.7 dB better than the traditional voltage mode biquad.

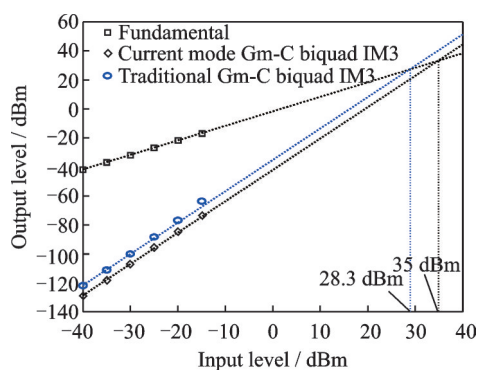


Fig.8 Comparison of IIP3 of current mode and traditional biquad

Besides, the current mode biquad only consumes 3.2 mW while the traditional one consumes 4.3 mW. The layout of the current mode biquad is shown in Fig.9 with a core area of  $0.06 \text{ mm}^2$ . Table 1 summarizes the simulated results of this paper and compares it with other state-of-the-art results in recent years. The figure of merit (FoM) used in Table 1 is shown in Eq.(7). Thanks to the proposed current mode Gm-C structure, this paper has the highest speed of 5 GHz, the smallest core area and the best FoM value with very good linearity and noise performances. Accordingly, the proposed current mode Gm-C filter is very suitable for broadband applications with high area-efficiency.

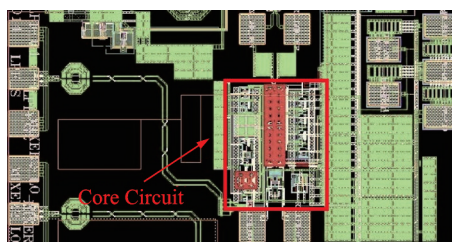


Fig.9 Layout of the filter

**Table 1 Performance comparison with other Gm-C filters**

Reference	[12]	[13]	[19]	[20]	Ours
Process					
CMOS/ nm	90	40	65	28	65
Topology	Gm-C	Active RC	Current mode	Current mode	Current mode
Order	2	4	4	2	2
SFDR/ dB	0	46	70.43		60
$f_c$ /GHz	1.114	1.6	0.0028	1	5
Gain/dB	2.37	10	-1	-1.8	2.5
IIP3/dBm		11.3	35.6	16	35
NF/dB					13.3@ 5 GHz
Area/mm <sup>2</sup>		0.12	0.5	0.374	0.06
$V_{DD}$ /V	0.6	1.1	2.5	1.5	2.5
Power/ mW	1.55	17.6	1.26	0.36	3.2
FoM/pJ	0.69	0.013	0.03		0.0003

$$\text{FoM} = \frac{\text{power}}{N_{\text{poles}} \times f_c \times \text{SFDR}} \quad (7)$$

where  $N_{\text{poles}}$  is the number of the poles and  $f_c$  the cut-off frequency. SFDR denotes spurious free dynamic range.

## 4 Conclusions

A 5 GHz wideband current mode second order filter is presented. By using of a current reused source degeneration OTA, the proposed filter can achieve much better noise and higher linearity performance with a lower power consumption compared with the traditional voltage mode filter. This paper is designed in standard 65 nm CMOS technology with a simulated IIP3 of 35 dBm and a power consumption of 3.2 mW.

## References

- [1] Base Station (BS) Radio Transmission and Reception (FDD). 3rd generation partnership project (3GPP) : TS 25.104, v.6.8.0[S]. [S.l.]: FDD, 2004.
- [2] CROLS J, STEYAERT M. Low-IF topologies for high-performance analog front ends of fully integrated receivers[J]. IEEE Transactions on Circuits and Systems-II, 1998, 45(3): 269-282.
- [3] NAESS O, BERG Y. Tunable ultralow voltage transconductance amplifier and Gm-C filter[J]. IEEE International Symposium on Circuits and Systems (ISCAS), 2000, 1: 709-712.
- [4] SILVA-MARTINEZ J, ADUT J, ROCHA-PEREZ M, et al. A 60-mW 200-MHz continuous-time sev-

enth-order linear phase filter with on-chip automatic tuning system[J]. IEEE Journal of Solid-State Circuits, 2003, 38(2): 216-225.

- [5] KOLM R, ZIMMERMANN H. A 3rd-order 235 MHz low-pass Gm-C filter in 120 nm CMOS[C]//Proceedings of the 32nd European Solid-State Circuits Conference (ESSCIRC). [S.l.]: IEEE, 2006: 215-218.
- [6] OTLN A, CELMA S, ALDEA C. A 0.18  $\mu\text{m}$  CMOS 3rd-order digitally programmable Gm-C filter for VHF applications[J]. IEICE Transactions on Information and Systems, 2005, E88-D(7): 1509-1510.
- [7] LE-THAI H, NGUYEN H, NGUYEN H, et al. An IF bandpass filter based on a low distortion transconductor[J]. IEEE Journal of Solid-State Circuits, 2010, 45(11): 250-261.
- [8] HOUFRAF F, EGOT M, KAISER A, et al. A 65 nm CMOS 1-to-10 GHz tunable continuous-time low-pass filter for high-data-rate communications[J]. IEEE International Solid-State Circuits Conference (ISSCC), 2012: 362-364.
- [9] KANEKO T, KIMURA Y, HIROSE K, et al. A 76-dB-DR 6.8-mW 20-MHz bandwidth CT  $\Delta\Sigma$  ADC with a high-linearity Gm-C filter[C]//Proceedings of ESSCIRC Conference 2016: 42nd European Solid-State Circuits Conference. Lausanne, Switzerland: IEEE, 2016: 253-256.
- [10] WEI J, YAO Y, LUO L, et al. A novel nauta transconductor for ultra-wideband Gm-C filter with temperature calibration[C]//Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS). [S.l.]: IEEE, 2019: 1-4.
- [11] RAMESH N, GAGGATUR J S. A 0.6 V, 2nd order low-pass Gm-C filter using CMOS inverter-based tunable OTA with 1.114 GHz cut-off frequency in 90 nm CMOS technology[C]//Proceedings of the 34th International Conference on VLSI Design and 2021 20th International Conference on Embedded Systems (VLSI-D). [S.l.]: [s.n.], 2021: 305-309.
- [12] WU C, HSIEH J, WU C, et al. An 1.1 V 0.1-1.6 GHz tunable-bandwidth elliptic filter with 6 dB linearity improvement by precise zero location control in 40 nm CMOS technology for 5G applications[C]//Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS). Baltimore, MD, USA: IEEE, 2017: 1-4.
- [13] SU K. Analog filters[M]. 2nd ed. New York, NY, United States:[s.n.], 2010.
- [14] TOKER A, OZOGUZ S, CICEKOGLU O, et al. Current-mode all-pass filters using current differencing buffered amplifier and a new high-Q bandpass filter



- configuration[J]. IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, 2000, 47(9): 949-954.
- [15] SOULIOTIS G, PSYCHALINOS C. Current-mode linear transformation filters using current mirrors[J]. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55(6): 541-545.
- [16] PIROLA A, LISCIDINI A, CASTELLO R. Current-mode, WCDMA channel filter with in-band noise shaping[J]. IEEE Journal of Solid-State Circuits, 2010, 45(9): 1770-1780.
- [17] HWANG Y, OH J, PARK J, et al. An always-on 0.53-to-13.4 mW power-scalable touchscreen controller for ultrathin touchscreen displays with current-mode filter and incremental hybrid  $\Delta\Sigma$  ADC[C]//Proceedings of IEEE 45th European Solid State Circuits Conference (ESSCIRC). [S.l.]: IEEE, 2019: 313-316.
- [18] PINI G, MANSTRETTA D, CASTELLO R. Analysis and design of a 260-MHz RF bandwidth +22-dBm OOB-IIP3 mixer-first receiver with third-order current-mode filtering TIA[J]. IEEE Journal of Solid-State Circuits, 2020, 55(7): 1819-1829.
- [19] SOHAL K, MANSTRETTA D, CASTELLO R. A 2nd order current-mode filter with 14 dB variable gain and 650 MHz to 1 GHz tuning-range in 28 nm CMOS[C]//Proceedings of 2021 IEEE International Symposium on Circuits and Systems (ISCAS). [S.l.]: IEEE, 2021: 1-5.
- [20] SANSEN W. Analog design essentials[M]. 1st ed. [S.l.]: Springer, 2006.
- [21] CHAI Y, NIU X, HE L, et al. A 60-GHz CMOS broadband receiver with digital calibration, 20-to-75-dB gain, and 5-dB noise figure[J]. IEEE Transactions on Microwave Theory and Techniques, 2017, 65(10): 3989-4001.
- [22] BECHTHUM E, RADULOV G, BRIAIRE J, et al. A wideband RF mixing-DAC achieving  $\text{IMD} < -82$  dBc up to 1.9 GHz[J]. IEEE Journal of Solid-State Circuits, 2016, 51(6): 1374-1384.
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- Author contributions** Dr. WU Xu designed the work, simulated, made the layout, post-simulation and wrote the manuscript. Prof. LI Lianming contributed to the discussion, background of the study and revised the manuscript. All authors commented on the manuscript draft and approved the submission.
- Competing interests** The authors declare no competing interests.

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## 应用于通信系统中的 5 GHz 电流模低噪声 G<sub>m</sub>-C 滤波器

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**摘要:**高线性度低噪声滤波器是通信系统中不可缺少的关键电路。基于电流复用型源极退化运算跨导放大器 (Operational transconductance amplifier, OTA) 结构, 本文提出了一种适用于高速通信系统的 5 GHz 电流模低噪声 G<sub>m</sub>-C 滤波器。利用电流模滤波器的结构特点和电流复用型源极退化 OTA 的高能效和高线性度, 本文设计的滤波器可在低功耗条件下仍具有良好的噪声和线性度性能。该滤波器采用标准 65 nm CMOS 工艺, 核心面积为 0.06 mm<sup>2</sup>。仿真结果表明, 其工作带宽为 5 GHz, IIP3 为 35 dBm, 而功耗仅为 3.2 mW。

**关键词:**G<sub>m</sub>-C 滤波器; 低通滤波器; 电流模滤波器