Analysis of Drain Modulation for High Voltage GaN Power Amplifier Considering Parasitics

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Abstract: For high-voltage and high-power Gallium Nitride (GaN) power amplifiers, a drain modulation circuit with rapid rise and fall time is proposed in this paper. To decrease the rise and fall time, the high-side bootstrap drive circuit with an auxiliary discharge switch is proposed. The effect of the parasitics is analyzed based on calculation and the parallel bonding is proposed. The storage capacitance of power supply is calculated quantitatively to provide large pulse current. To ensure safe operation of the power amplifier, the circuit topology with the dead-time control and sequential control is proposed. Finally, a prototype is built to verify the drain modulation circuit design. The experiments prove that the rise time and fall time of the output pulse signal are both less than 100 ns.

Key words: drain modulation; GaN; high voltage; power amplifier; parasitic inductance; N-MOS driver

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0 Introduction

Pulsed solid-state amplifiers is replacing tubes in the fields of radar and wireless communications in recent years[1-2]. To further meet the growing demand for high power, high efficiency and wide bandwidth, Gallium Nitride high-electron mobility transistors (GaN HEMTs) as a typical example of the third-generation semiconductor devices has been applied[3-4]. Compared with the gate modulation, the drain modulation improves the heat dissipation of the power amplifier and is immune to slight fluctuations, which is widely applied[5-6].

However, the conventional drain modulation is 28 V and less than 30 A, whose rise/fall time is more than 200 ns[7]. For 80 V kW-level GaN pulsed power amplifier, the volume of the conventional P-type metal oxide semiconductor field effect transistor (P-MOS) drain modulation scheme is too large[8-9]. Besides, due to the narrow pulse width, the rise and fall time of less than 100 ns is essential, which can hardly satisfied with the traditional topology. Therefore, it is necessary to develop a reliable modulation circuit for high-voltage and large-current GaN power amplifiers.

1 Proposed Drain Modulation Circuit

Table 1 shows the specifications of the designed modulation circuit for the GaN power amplifier. The operating voltage is 80 V, the peak current is up to 160 A, and the rise and fall time should be less than 100 ns.

Table 1 Specifications of drain modulation circuit

Parameter	Value
Voltage V_{in}/ V	80
Input peak current I_p/ A	160
Rise time t_r/ ns	100
Fall time t_f/ ns	100

For traditional drain modulation circuit, the voltage is low and thus P-MOS is used[10-11]. Compared with P-MOS, the drive circuit of N-type met-

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al oxide semiconductor field effect transistor (N-MOS) is much more difficult[12-13]. Besides, the demanding rise/fall time and large peak current add to the difficulty of design.

As shown in Fig.1, a drain modulation circuit for high-voltage GaN power amplifiers is proposed. The circuit is composed of the power supply block, main switch block, discharge circuit block, control block and driver block.

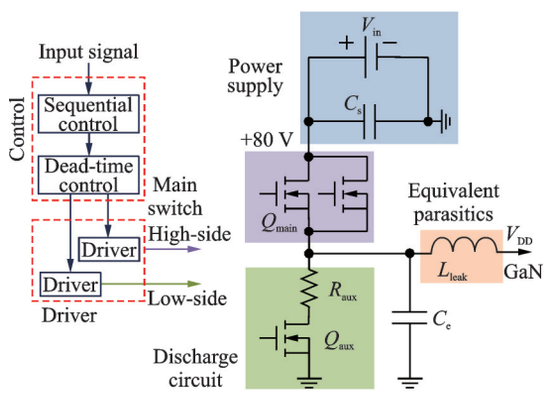


Fig.1 The proposed drain modulation circuit

To meet the rise and fall time demand of the output voltage V_{DD}, the proper driver chip and main switch Q_{main} for high voltage application are chosen based on theoretical calculation. To further decrease the fall time, an auxiliary switch Q_{aux} and auxiliary resistor R_{aux} are added to the drain modulation circuit as the discharge circuit. The influence of the parasitic inductance L_{leak} and stabilizing capacitor C_e are analyzed, and the parallel bonding is proposed to reduce the parasitic influence, which can optimize the rise and fall time. Besides, to minimize the voltage overshoot caused by the parasitics, the storage capacitance C_s is designed. As to the control law, the time sequential control and dead-time control are designed with discrete devices to ensure proper operation of the power amplifier.

2 Design of Drive Circuit

The turn-on and turn-off procedure is shown in Fig.2. During the turn-on process, the gate drive current I_{g_on} charges the capacitance C_{gs} and C_{gd}. During the turn-off process, the gate drive current I_{g_off} discharges the capacitance C_{gs} and C_{gd}. To achieve faster rising and falling edge, increasing driving current is the first priority.

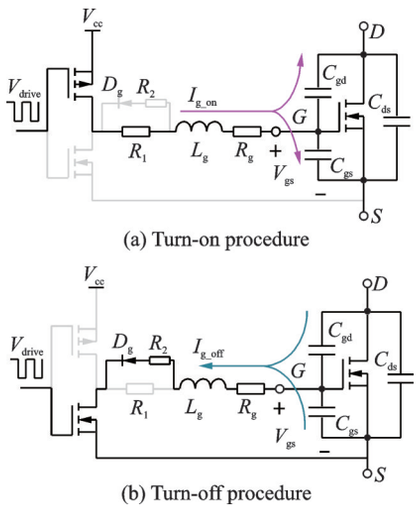


Fig.2 Turn-on and turn-off procedure

The approximate switching time can be calculated as

$$t_{switch} = \frac{Q_{gs} + Q_{gd}}{I_g} \tag{1}$$

where Q_{gs} is the gate to source charge, Q_{gd} the gate to drain charge, and I_g the gate drive current.

It can be seen that the switching time depends on the intrinsic characteristics of the main switch and the gate drive current. To decrease the switching time, the gate charge of the chosen main switch should be small and the gate drive current should be as large as possible.

Even a large-current driver is chosen, the fall time can still be large due to the charging process of C_{ds}. To further decrease the fall time, an auxiliary branch with a switch and resistor is proposed as the discharge circuit to provide a low-impedance discharge loop. Fig.3 compares the fall time between the conventional topology and the proposed topology. It can be seen that the fall time is decreased dramatically from 62 ns to 6 ns with the proposed topology when the load is 50 Ω.

In addition, a bootstrap structure is adopted for high voltage N-MOS driving circuit. When the main switch is turned off, the boot capacitor is charged to the supply voltage V_{cc} through the bootstrap charge loop shown in Fig.4. When the main switch Q_{main} is turned on, the boot capacitor C_b provides the level-shifted voltage. The bootstrap diode D_b should be fast recovery, especially when the switching frequency is high.

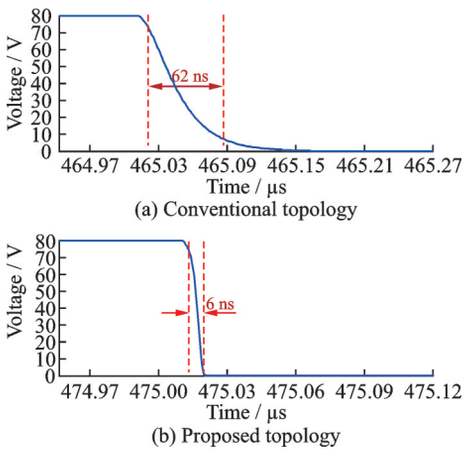


Fig.3 Comparison of fall time between different topologies

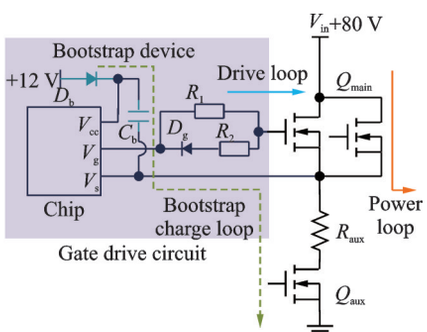


Fig.4 Boot-strap drive circuit for the main switch

To provide enough charge during the high-side drive cycle, the bootstrap capacitance C_B should satisfy the following equation

$$C_B \geqslant \frac{Q_g + t_{max} \cdot I_B}{\Delta V_{CB}} \tag{2}$$

where Q_g is the total gate charge for Q_{main}, t_{max} the maximum time when Q_{aux} is off, and ΔV_{CB} the allowable ripple.

The bootstrap resistor R_B is to limit inrush current at startup, and the resistance is

$$R_B \geqslant \frac{t_{min}}{3C_B} \tag{3}$$

where t_{min} is the minimum time when Q_{aux} is on.

The peak current of the diode I_{pk} should be

$$I_{pk} \geqslant \frac{V_{DD} - V_F}{R_B} \tag{4}$$

where V_{DD} is the supply voltage, and V_F the diode forward voltage drop.

3 Analysis Considering Parasitics

The parasitics induced by printed circuit board (PCB) layout and bonding are unavoidable. As a result, the output voltage drop and even oscillation are caused. To ensure the rise and fall time of the drain modulation circuit, the effect of the parasitics is analyzed and the parallel bonding is proposed to minimize the parasitic inductance. The storage capacitance of the power supply is designed to decrease the output voltage drop.

3.1 Parasitic inductance analysis

Typically, the radio-frequency (RF) circuit and the drain modulation circuit are bonded by the terminals, which induces the parasitics. Therefore, the rising and falling edge are affected seriously. To optimize the output characteristics of the proposed drain modulation circuit, the influence of parasitics analyzed and simulated.

The equivalent circuit of the proposed circuit is shown in Fig. 5. where C_{oss} is the parasitic capacitance of Q_{main} and R_o is the load.

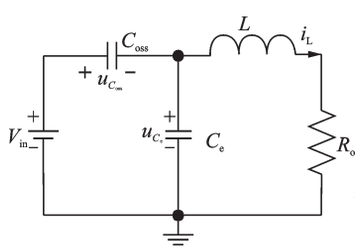


Fig.5 Equivalent circuit

The output voltage V_{DD} can be analyzed and calculated as follows. Apply Kirchhoff's voltage law (KVL) and Kirchhoff's current law (KCL) to the equivalent circuit

$$L\frac{di_L(t)}{dt} + R_o \cdot i_L(t) = u_{C_e}(t) \tag{5}$$

$$i_L(t) + C_e\frac{du_{C_e}(t)}{dt} = C_{oss}\frac{du_{C_{oss}}(t)}{dt} \tag{6}$$

where $i_L(t)$ is the parasitic inductance current, $u_{C_e}(t)$ the voltage of C_e, and $u_{C_{oss}}(t)$ the voltage of C_{oss}.

Combine above the equations and differentiate both sides of the equation

$$Li_L''(t) + R_o \cdot i_L'(t) + \frac{1}{C_{oss} + C_e} i_L(t) = 0 \tag{7}$$

where $i_L''(t)$ is the double-differentiation of $i_L(t)$, and $i_L'(t)$ the differentiation of $i_L(t)$.

Taking the Laplace transform of Eq. (7), we have

$$s^2 LI_L(s) - \frac{sLV_{in}}{R_o} + sR_o I_L(s) - V_{in} + \frac{I_L(s)}{C_{oss} + C_e} = 0 \tag{8}$$

$I_L(s)$ can be solved as

$$I_L(s) = \frac{sLV_{in}/R_o + V_{in}}{s^2 L + sR_o + 1/C_{oss} + C_e} \tag{9}$$

Take the inverse Laplace transform, and $i_L(t)$ is

$$i_L(t) = \frac{R_o V_{in} e^{-\frac{R_o t}{2L}} \sinh(mt) + 2mLV_{in} e^{-\frac{R_o t}{2L}} \cosh(mt)}{2mLR_o} \tag{10}$$

where the expression of constant m is

$$m = \sqrt{\frac{C_e R_o^2 - 4L + C_{oss} R_o^2}{4C_e L^2 + 4C_{oss} L^2}} \tag{11}$$

So the output voltage $V_{DD}(t)$ is

$$V_{DD}(t) = \frac{R_o V_{in} e^{-\frac{R_o t}{2L}} \sinh(mt) + 2mLV_{in} e^{-\frac{R_o t}{2L}} \cosh(mt)}{2mL} \tag{12}$$

With Eq.(12), the relationship between the output voltage V_{DD} and the parasitic components of the drain modulation circuit can be known. The rise and fall time and the output oscillation are affected by the parasitics.

Comparing the output voltage waveforms with different parasitics by simulation, the schematic diagram is shown in Fig.6. The power supply voltage of the simulated circuit is 80 V, the storage capacitance is 200 μF and the load is 1.5 Ω. The stabilizing capacitor is equivalent to C_e. Small C_e may cause oscillation and instability of the power amplifier. The parasitic inductor is equivalent to L_{leak}.

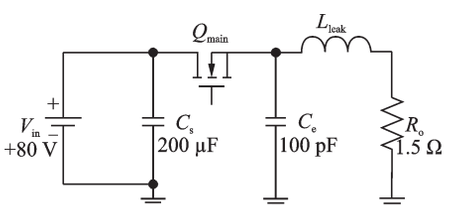


Fig.6 Schematic diagram of simulation

Setting C_e as 100 pF, and the simulation results are compared with the parasitic inductance of 0.5, 2, 3.5 and 5 nH. The simulated waveforms are shown in Fig.7.

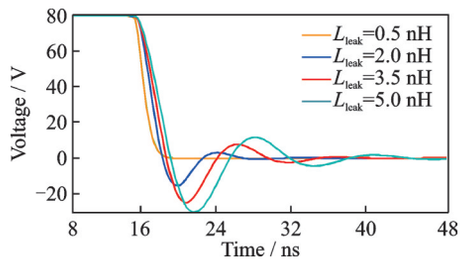


Fig.7 Simulated output voltage with different L_{leak}

When the parasitic inductance is small, such as 0.5 nH, the output voltage is perfect and there is no oscillation. As the parasitic inductance increases, the output voltage tends to oscillate when the input signal of the drain modulation circuit is at low level. The oscillation can lead to the disruption of the power amplifier output, and thus should be minimized.

So, the bonding procedure should be controlled to minimize the parasitic inductance, such as parallel bonding wires. The output characteristics can be studied according to Eq.(12) to determine the range of parasitics during design stage.

The value of capacitance C_e for stability should be chosen carefully as well. When C_e is too small, the power amplifier would be unstable, as shown in Fig.8(a). But when C_e is too large, the falling edge would be too slow and the drain modulation circuit still operates without the input signal, as shown in Fig.8(b).

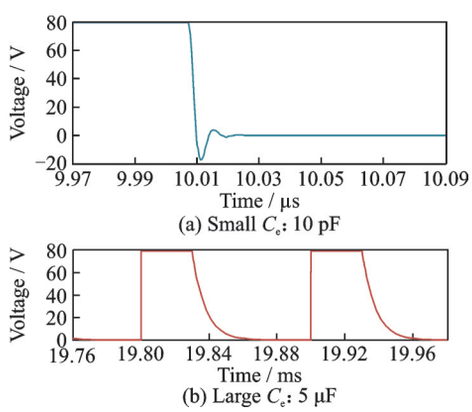


Fig.8 Simulated output voltage with different C_e (L_{leak}= 2 nH)

3.2 Storage capacitor design

Due to the limited DC voltage source and parasitic inductive effect, the output voltage drops when the drain current changes dramatically. To keep the output voltage, the direct current power source

should be designed according to the peak current. However, the volume is seriously increased and unnecessary power loss is produced under this condition. Another method is to design the storage capacitor C_s properly to provide the instantaneous large current.

The storage capacitor is charged to V_{in} by the DC voltage source when the power amplifier does not operate. Since the needed current during the pulse is provided by the storage capacitor, the voltage of the power amplifier V_{DD} is

$$V(t) = V_{in} - \frac{1}{C_s}\int i(t)\,dt \tag{13}$$

Express the voltage drop ratio σ as

$$\sigma = \frac{\Delta V}{V_{in}} = \frac{1}{C_s V_{in}}\int i(t)\,dt \tag{14}$$

Assuming that the drain current is constant during the pulse, then the designed storage capacitance can be calculated according to the following equation.

$$C_s = \frac{I_p \cdot T}{V_{in} \cdot \sigma} \tag{15}$$

where I_p is the peak current and T the pulse width.

As to the implementation of the storage capacitor, the tantalum capacitors or electrolytic capacitors with high value are selected. However, their withstand voltage is low. To meet the requirements of 100 V high voltage, two capacitors are connected in series. Moreover, the parasitic inductance and resistance of these polarity capacitors (C_2—C_5) are usually large, which can cause the increase of rise time of the output modulation signal. To solve the problem, a ceramic capacitor with the small parasitics C_1 is connected to the polarity capacitors in parallel, as shown in Fig.9.

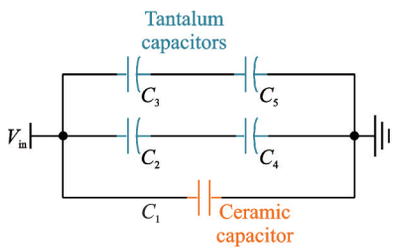


Fig.9 Implementation of storage capacitor

4 Proposed Control Circuit

Without proper control circuit, the whole system would break. Since GaN power amplifier can burn up without negative gate voltage, additional sequential circuit is critical for operation. Besides, to prevent shoot-through of the main switch and the auxiliary switch, a dead-time control is implemented. The control block diagram is shown in Fig.10.

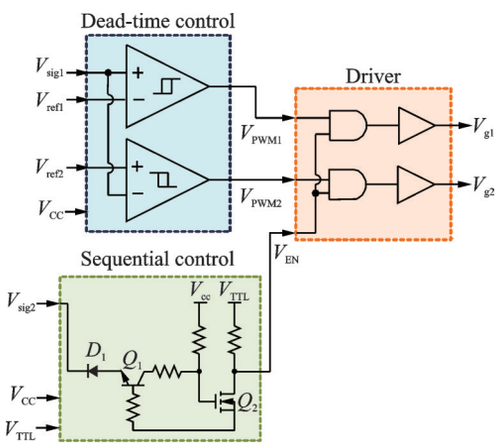


Fig.10 Control block diagram

4.1 Sequential circuit design

There are strict sequence restrictions when the GaN power amplifier is powered on. When the gate voltage of the depletion GaN HEMT is zero, the drain current is very large, which can lead to the failure of GaN device. So, the drain voltage should be applied only when the gate voltage of the GaN HEMT is negative. And the power-off sequence is the opposite. Therefore, it is necessary to design a sequential control circuit for protection, as shown in Fig.11. With the proposed sequential control circuit, there would be no drain voltage without negative gate voltage of GaN.

The principle of the sequential control circuit is

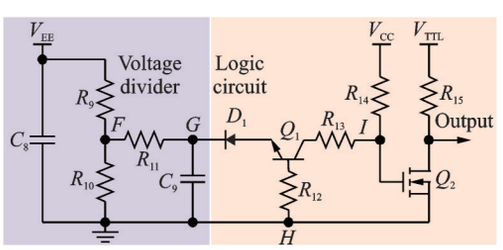


Fig.11 Sequential control circuit

as follows. When the gate voltage of the GaN power amplifier V_{EE} is negative, the voltage V_F is also negative. When the base to emitter voltage V_{be} of the triode is greater than the threshold voltage, Q_1 is turned on. The voltage V_I is

$$V_I = V_G + V_{D1} + V_{Q1} + V_{R13} \approx V_G \quad (16)$$

So the gate to source voltage of Q_2 is negative, and Q_2 is turned off. Under this condition, the output voltage is V_{TTL} and the proposed drain modulation circuit works, as shown in Fig.12(a). Similarly, as shown in Fig.12(b), when the gate voltage of the GaN power amplifier is zero, Q_1 is off and Q_2 is on. Therefore, the output voltage is 0, and the modulation circuit would not work.

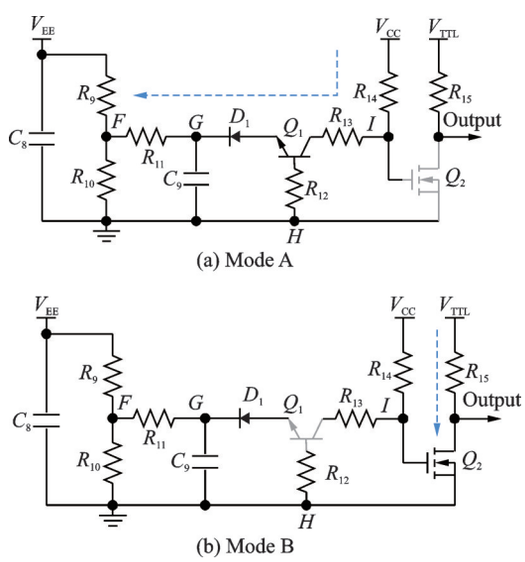


Fig.12 Operation modes of the proposed sequential circuit

Based on above analysis, the designed sequential control circuit ensures the proper sequence of the GaN power amplifier.

4.2 Dead-time control design

To prevent failure caused by the shoot-through, a dead-time control is applied to the main switch Q_{main} and the discharge switch Q_{aux}. The dead-time control circuit is shown in Fig.13, which consists of two voltage dividers, two RC delay circuits, a non-inverting hysteresis comparator and an inverting hysteresis comparator.

Assuming that two threshold voltages of the hysteresis comparators are V_L and V_H. When the

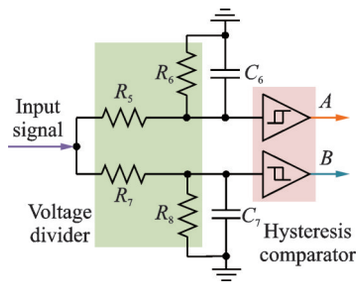


Fig.13 Dead-time control circuit

output voltage of the hysteresis comparator jumps to high level, the input threshold voltage is

$$V_{TH1} = V_L(R_5 + R_6)/R_6 \quad (17)$$

Similarly, when the output voltage jumps from high level to low level, the input threshold voltage is

$$V_{TH2} = V_H(R_5 + R_6)/R_6 \quad (18)$$

For the inverting hysteresis comparator, the input threshold voltages can be derived in the same way. As shown in Fig.14, the dead-time control is realized by the voltage difference between V_{TH2} and V_{TH4}, and V_{TH1} and V_{TH3}.

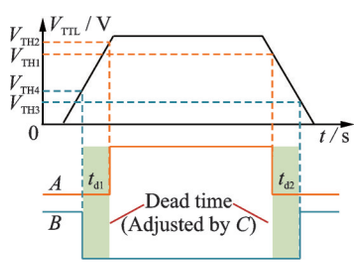


Fig.14 Waveforms of the dead-time control

To adjust the dead-time, the capacitance C_6 and C_7 is changed. And the dead time can be calculated as

$$t_{d1} = R_7C_7 \ln\left(1 - V_H\frac{R_7 + R_8}{V_{TTL}R_8}\right) - R_5C_6 \ln\left(1 - V_H\frac{R_5 + R_6}{V_{TTL}R_6}\right) \quad (19)$$

$$t_{d2} = R_7C_7 \ln\left(V_L\frac{R_7 + R_8}{V_{TTL}R_8}\right) - R_5C_6 \ln\left(V_L\frac{R_5 + R_6}{V_{TTL}R_6}\right) \quad (20)$$

5 Efficiency of the Proposed Topology

5.1 Power amplifier

Power amplifiers are classified into linear pow-

er amplifiers such as Class A, Class B and Class C, and nonlinear power amplifiers such as Class D, Class E and Class F[14-15]. The nonlinear power amplifiers have significantly higher efficiency than the classical linear power amplifiers[16-17].

An overview of the ideal performance of different types of power amplifiers is shown in Table 2, where δ is the waveform factor, η the efficiency and P_{max} the power output capability. Considering the overall efficiency, the nonlinear amplifier classes are preferred.

Table 2 Performance of common amplifiers[18]

Class	δ	η	P_{max}
A	2	0.5	0.125
B	2	0.78	0.125
E	3.54	1	0.098
F	2	1	0.159

5.2 Power supply

The loss of the drain modulation circuit is mainly decided by the main switch, which includes the driving loss, the switching loss and the conduction loss[19]. The loss is calculated by the following equations

$$P_g = V_g \cdot Q_g \cdot f_s \tag{21}$$

$$P_{switch} = \frac{V_{ds} \cdot I_Q}{2} \cdot \frac{Q_{gs} + Q_{gd}}{I_g} \cdot f_s \tag{22}$$

$$P_{on} = R_{dson} \cdot I_Q^2 \tag{23}$$

where P_g is the driving loss, V_g the driving voltage, f_s the switching frequency, P_{switch} the switching loss, P_{on} the conduction loss, R_{dson} the on-resistance of the switch and I_Q the switch current.

The total loss of the drain modulation circuit is

$$P_{loss} = P_g + P_{switch} + P_{on} \tag{24}$$

The individual loss obtained from Eqs.(21—23) is shown in Fig.15. It is noted that the maximum loss is the conduction loss, and thus the increased voltage of 80 V can dramatically decrease the overall loss. The conduction loss of 80 V is only 14% of the conduction loss of 30 V. So, the increased input voltage is significant for miniaturization.

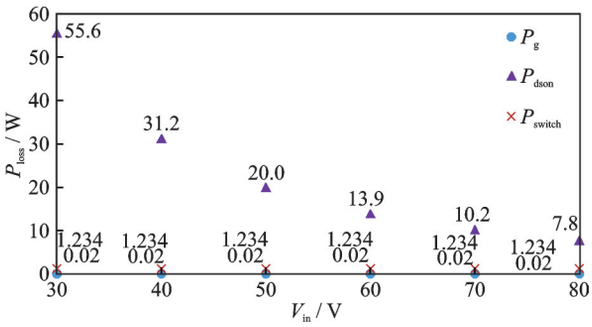


Fig.15 Calculated loss(V_{in}=80 V, f_s=10 kHz)

6 Experimental Results

In order to verify the proposed drain modulation circuit, a prototype is built, as shown in Fig.16. The tantalum capacitors and the ceramic capacitors are connected in parallel to serve as the storage capacitor. The main switch is the 100 V N-MOS from Infineon.

The results of the output signal are shown in Fig.17. It can be seen that the rise time and fall time of the output pulse signal are both less than 100 ns,

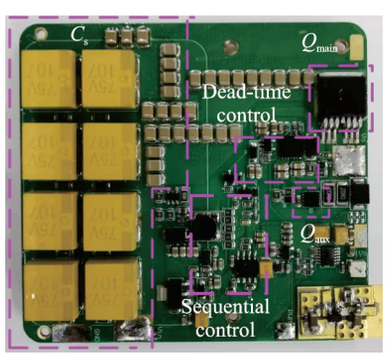
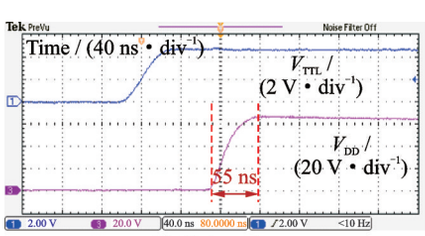
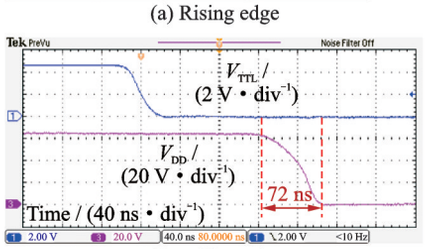


Fig.16 Prototype of the proposed drain modulation circuit



(a) Rising edge



(b) Falling edge

Fig.17 Experimental waveforms

which satisfies the requirements.

The comparison of different modulation schemes is shown in Table 3. Compared with the gate modulation, the reliability of the proposed drain modulation circuit is high, the rise and fall time are small, and the power amplifier loss in standby is small.

Table 3 Comparison of different modulation schemes

Categories of modulation strategy	Reliability	Rise/ fall time	Static loss
Gate modulation	Low	Small	Large
Drain modulation	High	Large	Small
The proposed method	High	Small	Small

7 Conclusions

A drain modulation circuit with rapid rise and fall time for 80 V kW level GaN power amplifier is proposed. The drive circuit including a bootstrap structure is adopted for high voltage N-MOS. To further decrease falling edge, an auxiliary switch is added as the discharge circuit. The effect of the parasitic inductance on the rise and fall time is analyzed and the parallel bonding is proposed to minimize the parasitics. The capacitors are selected according to the derived equations to decrease voltage drop and oscillation. As to the control law, a sequential control circuit with discrete components is designed to ensure proper sequence of gate voltage and drain voltage for the power amplifier, and a dead-time control circuit composed of hysteresis comparator is added to prevent shoot-through. Finally, an 80 V prototype is built. The rise time is 55 ns and the fall time is 72 ns, which can satisfy the requirement of less than 100 ns.

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考虑寄生参数的高压GaN功率放大器漏极调制电路分析

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摘要：提出了一种适用于高压高功率GaN功率放大器的漏极调制电路。采用高压自举驱动电路并增加泄放开关管的方式以减小上升时间和下降时间。基于对寄生参数影响的分析及计算，提出了并联加电线的措施。此外，定量计算了提供脉冲大电流所需的储能电容容值。为了确保功率放大器的安全运行，提出了死区控制电路及时序控制电路。搭建了一台实验样机验证所提漏极调制电路设计的有效性，实验结果表明该样机的上升时间和下降时间均小于100 ns。

关键词：漏极调制；氮化镓；高压；功率放大器；寄生电感；N-MOS驱动