Optimal Control for Vienna Rectifier in Unbalanced Conditions

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Abstract: The Vienna rectifier is a widely adopted solution for high-power rectification due to its efficiency and straightforward design. However, its performance can degrade under unbalanced three-phase voltage conditions, leading to current zero-crossing distortion and compromised dynamic response. This paper investigates the causes of these distortions, identifying a phase shift between the input current and the grid voltage as a primary factor, and proposes an effective distortion phase identification strategy. Furthermore, the dynamic performance is enhanced through improved current reference calculations and a refined power feedforward strategy. This approach optimizes the system's response to load changes and maintains output voltage stability under unbalanced conditions. Simulation results validate the effectiveness of the proposed methods in reducing current distortion and improving overall performance.

Key words: zero-crossing distortion; three-phase voltage unbalanced; rectifier; power feedforward

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0 Introduction

In scenarios such as electric vehicle fast charging stations and data centers, there is a significant presence of direct current (DC) loads, while the power supply originates from a three-phase alternating current (AC) power grid. Consequently, high-power and highly reliable rectifiers are required to achieve the AC-to-DC conversion. In this context, various three-phase rectifier topologies have been developed, such as diode-clamped three-level PWM rectifiers, flying capacitor three-level PWM rectifiers, and Vienna rectifiers[1-3]. Among these, the Vienna rectifier is distinguished by its high reliability, relatively simple circuit topology, and lower implementation cost, making it widely adopted in various applications. Therefore, it has become a prominent subject of extensive research and development.

Current research primarily focuses on aspects such as current control algorithms, modulation techniques, and DC side voltage balance control[4-5], typically assuming an ideal power grid as the input. To accommodate grid fluctuations and complex power supply environments, it is essential to address the stable operation of the Vienna rectifier under conditions of unbalanced three-phase voltage[6]. Under unbalanced grid conditions, the Vienna rectifier experiences power fluctuations due to input voltage asymmetry, leading to oscillations in the output voltage. To enhance control strategies, it is essential to segregate positive and negative sequence components for individual regulation[7] or to improve coordinate transformation[8] for better voltage control. When faced with unbalanced input voltages, the Vienna rectifier loses synchronization between the input current and the grid voltage, which leads to power oscillations and consequently causes variations in the DC output voltage.

However, discrepancies between the Vienna rectifier's input current and the grid voltage may

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lead to modulation irregularities and current zero-crossing distortion[9]. Addressing zero-crossing distortion requires precise evaluations of phase disparities and timing, utilizing clamping modulation waves to minimize current distortion[10-11]. Nevertheless, thorough assessments for zero-crossing compensation increase computational complexity due to control methods based on positive and negative sequence separation, which diminishes the practicality of this approach. Furthermore, incorporating load current feedforward[12] within the control loop enhances system dynamics by enabling quick adaptation to load changes, thereby maintaining output voltage stability. The challenge lies in ensuring the input power reference responds in real time to load changes. In balanced three-phase scenarios, merely forwarding the d-axis load current suffices. However, under unbalanced conditions, relying solely on the positive sequence d-axis load current will result in inaccuracies, impair dynamic performance, and compromise output voltage stability.

To address the control issues under the aforementioned unbalanced conditions, this paper proposes an optimized control strategy. The effectiveness of the proposed methods is verified through simulations under both steady-state and dynamic load conditions, including various levels of grid voltage imbalance. Notably, even with a 60% voltage drop in one phase, the proposed method maintains stable operation. Despite slight overmodulation, current quality is significantly improved. Compared with traditional positive-negative sequence separation methods, the proposed approach reduces computational complexity and is easier to implement. Additionally, the load feedforward strategy enhances the dynamic response, maintaining output voltage stability during load transients.

The paper is organized as follows: Section 1 elaborates on the operational principles of the Vienna rectifier under balanced grid conditions, followed by an in-depth analysis of current zero-crossing distortion phenomena and corresponding detection methodologies. Section 2 systematically presents the current reference calculation framework under unbalanced voltage conditions, while introducing a novel dynamic response enhancement strategy to improve transient performance. Section 3 demonstrates comprehensive simulation studies validating the proposed approaches, and Section 4 provides experimental verification through hardware implementation.

1 Causes of Current Zero-Crossing Distortion and Identification Methods

1.1 Principle of Vienna rectifier under three-phase balanced conditions

The primary control objectives of the Vienna rectifier are the regulation of the DC voltage and the correction of the power factor. When the grid voltage becomes unbalanced, the operating state of the rectifier will change accordingly. To further analyze this process and elucidate the causes of zero-crossing distortion, the following sections will first present the fundamental structure and operational principles of the Vienna rectifier under balanced conditions.

The main circuit topology of the Vienna rectifier is illustrated in Fig.1. This topology includes boost inductors L_a, L_b, L_c on the AC side, diodes D_1—D_6, bidirectional switches S_a, S_b, S_c, and filtering capacitors C_1 and C_2 on the DC side. In this arrangement, D_1, D_4, S_a, D_3, D_6, S_b, along with D_5, D_2, and S_c, collectively form the a, b, and c three-phase bridges. Each switch S_a, S_b, S_c consists of two switch devices connected in series in a reverse configuration, with one terminal connected to the midpoint of each phase bridge (a, b, c) and the other terminal connected to the midpoint M of the

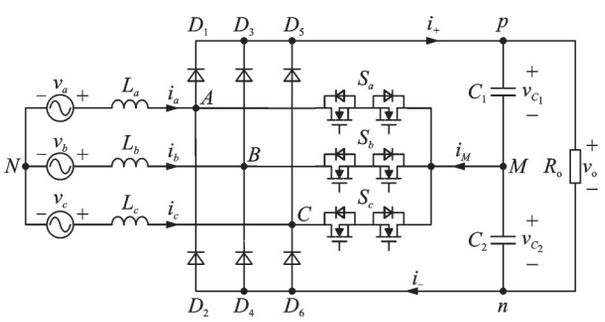

Fig.1 Main circuit topology of the Vienna rectifier

two DC side filtering capacitors. v_a, v_b, v_c represent the three-phase supply voltages, while v_o denotes the output voltage. R_o signifies the load resistance. i_+ and i_- are the currents from bridge to the capacitor and i_M is the current from swatches to the middle point of capacitors.It is specified that the direction of the three-phase input currents in Fig.1 is defined as the positive direction.

Under stable operating conditions, the midpoint between the AC and DC sides of the Vienna rectifier only contains fundamental frequency components. Therefore, this circuit can be considered as three single-phase circuits combined. To facilitate the explanation of its working principle, it can be assumed that the voltage between the AC and DC measurement points M and N is zero, which effectively achieves three-phase decoupling. This assumption allows for the examination of the individual voltage vector relationships of the single-phase circuits. Fig.2 illustrates the vector relationship diagram of the phase voltage for phase a. δ is the phase angle between the grid voltage and the voltage v_{AM}, which is the voltage from point A to point M. It is evident that the grid voltage and the voltage waveforms of the switches v_{AM} together determine the inductor voltage. Since the grid voltage is an uncontrollable input variable, the inductor voltage can be regulated by adjusting the voltage of the switches, thereby influencing the inductor current. Considering the phase voltage differences among the three phases and the midpoint potential difference v_{MN} between the AC and DC sides, the following equation can be formulated as

$$\begin{cases} L\dfrac{\mathrm{d}i_a}{\mathrm{d}t} = v_a - v_{AN} = v_a - v_{AM} - v_{MN} \\ L\dfrac{\mathrm{d}i_b}{\mathrm{d}t} = v_b - v_{BN} = v_b - v_{BM} - v_{MN} \\ L\dfrac{\mathrm{d}i_c}{\mathrm{d}t} = v_c - v_{CN} = v_c - v_{CM} - v_{MN} \end{cases} \tag{1}$$

where L is the inductor value of L_a, L_b and L_c. v with different capital subscripts denote the voltage difference between two points. For example, v_{AM} represents the voltage from point A to point M, and then we get

$$v_{AM} = \frac{v_{AM} + v_{BM} + v_{CM}}{-3} \tag{2}$$

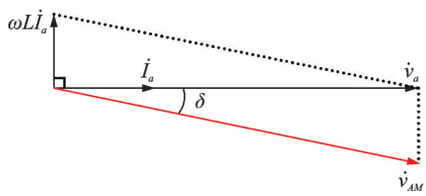

Fig.2 Voltage vector diagram of phase a

According to the analysis above, the fundamental component of the three-phase switch voltages are all sinusoidal waveforms with a phase difference of 120°, and fundamental component of v_{MN} is zero, which is consistent with the analysis above. Therefore, as long as the analysis and modulation of the switch voltages can be determined, the current closed-loop control can be achieved.

As the voltage across the switches is influenced by their states and the voltages at the midpoint of the rectifier bridge, it is essential to integrate this with the modulation approach for analysis. When the switches are conducting, the voltage across them is zero. Conversely, when the switches are turned off, their voltage depends on the direction of the input current: When the input current is positive, it flows through the upper diode, resulting in the voltage across the switches being equal to the upper capacitor voltage, which is $v_o/2$; When the input current is negative, it flows through the lower diode, causing the voltage across the switches to be the lower capacitor voltage, which is $-v_o/2$.

Under balanced three-phase conditions with a power factor of 1, as previously mentioned, the current phase is the same as the grid voltage. The voltage drop across the inductor due to current flow is minimal, indicating that the grid voltage (current) is in phase with the switch voltages. If a reverse cascaded carrier modulation method is employed, the modulation principle dictates that the ratio of the fundamental component in the diagram to the modulation wave amplitude is K_{PWM}. Consequently, the regulation of the current in phase a can be considered as being achieved through the control of the modulation wave v_{Ma}, which also applies to the other two phases.

1.2 Causes and identification methods of zero-crossing distortion

As mentioned earlier, controlling the modulation wave adjusts the fundamental component of the switch voltages, which helps regulate the inductor voltage and control the input current. However, this analysis assumes that the current phase matches the grid voltage. When the three-phase voltages are unbalanced, we need to recalculate the input current to maintain constant instantaneous power and prevent voltage fluctuations at the output.

Under unbalanced conditions, the input current may not be in phase with the modulation wave, making the previous analysis invalid, as shown in Fig.3, where i_{a_ref} is the reference of current of phase a, v_{Ma} the modulation wave and V_o the steady-state value of the output voltage v_o. This mismatch can cause significant distortions in the input current, lowering the power factor and leading to output voltage fluctuations. Additionally, these current distortions affect the modulation wave during current loop adjustments. As a result, the voltages across the switches will be opposite to the original PWM levels, further worsening distortions in the other phase currents.

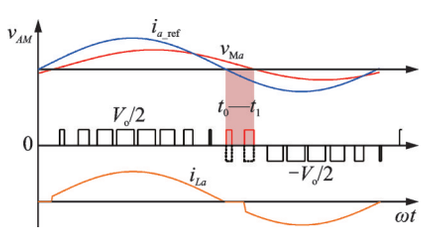

Fig.3 Current waveform diagram under unbalanced condition

Based on the previous analysis, the phase shift between the current reference and the modulation wave causes modulation errors. While calculating this phase shift and adjusting the modulation wave to prevent current distortion is feasible, the process is complex and demands significant computational resources. To simplify the process, the signs of the current reference and the modulation wave can be directly assessed. By injecting the modulation wave with opposite signs as zero-sequence values into the three-phase modulation wave, compensation for zero-crossing distortion can be achieved. If the current is in a distorted region, the modulation wave phase can be clamped to zero, ensuring that the switches remain continuously on, allowing the current to naturally cross zero without distortion which shown in Fig.4.

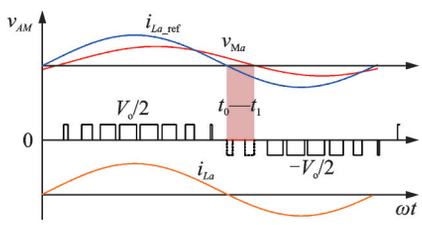

Fig.4 Current waveform with compensation

Thus, effective clamping is enabled by determining the polarity of the modulation wave relative to the actual current. It is important to note that if one phase is distorted and the modulation wave is clamped, the modulation waves of the other two phases should be adjusted similarly. This ensures that the zero-sequence component is consistently applied to the three-phase modulation wave during clamping, preventing distortions in the currents of the other phases, as shown in Fig.5. v_{M0} means the zero-sequence modulation component.

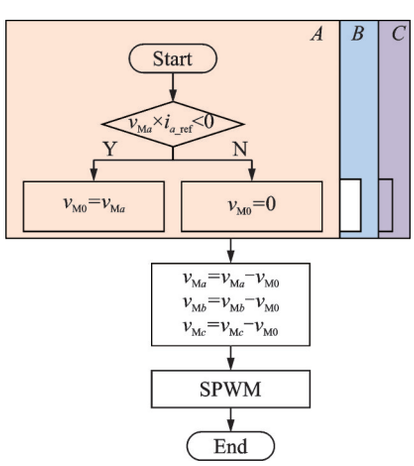

Fig.5 Distortion detection and modulation wave compensation

2 Improvement Methods for Dynamic Response Under Unbalanced Grid Conditions

2.1 Calculation of current reference and power feedforward method

Under balanced three-phase conditions, a load

current feedforward method is employed to enhance the system's dynamic response to load fluctuations. This method feeds the load current forward to the current reference, enabling the input power to quickly match the output power and ensuring output voltage stability. The feedforward value serves as the d-axis current reference, aligning with its physical significance, as shown in Fig.6.

However, when the three phases are unbalanced, the current reference is divided into positive and negative sequence dq references. Consequently, feeding the load current forward to the d-axis current introduces errors, diminishing the effectiveness of the feedforward method in improving dynamic performance and leading to steady-state errors. To facilitate analysis, the power expression under unbalanced conditions is first provided as

$$\begin{bmatrix} P_{\text{in}} \\ Q_{\text{in}} \\ P_{\text{in2}} \\ P_{\text{in2}} \end{bmatrix} = \begin{bmatrix} v_{dp} & v_{qp} & v_{dn} & v_{qn} \\ v_{qp} & -v_{dp} & -v_{qn} & v_{dn} \\ v_{qn} & -v_{dn} & -v_{qp} & v_{dp} \\ v_{dn} & v_{qn} & v_{dp} & v_{qp} \end{bmatrix} \begin{bmatrix} i_{dp} \\ i_{qp} \\ i_{qn} \\ i_{dn} \end{bmatrix} \tag{3}$$

where "in" denotes the DC component of the output power, "in2" the secondary component of the input power, "dp" the positive sequence d-axis component, "dn" the negative sequence d-axis component, "qp" the positive sequence q-axis component, and "qn" the negative sequence q-axis component. During control, an appropriate current reference must be calculated to eliminate pulsating components, ensuring that the input power consists solely of the DC component P_{in}.

When the three phases are unbalanced, the formula for calculating the current reference is

$$\begin{bmatrix} i_{dp\_\text{ref}} \\ i_{qp\_\text{ref}} \\ i_{dn\_\text{ref}} \\ i_{qn\_\text{ref}} \end{bmatrix} = \begin{bmatrix} v_{dp} & v_{qp} & v_{dn} & v_{qn} \\ v_{qp} & -v_{dp} & -v_{qn} & v_{dn} \\ v_{qn} & -v_{dn} & -v_{qp} & v_{dp} \\ v_{dn} & v_{qn} & v_{dp} & v_{qp} \end{bmatrix}^{-1} \begin{bmatrix} P_{\text{ref}} \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{4}$$

The current reference expression can be solved as

$$\begin{bmatrix} i_{dp\_\text{ref}} \\ i_{qp\_\text{ref}} \\ i_{dn\_\text{ref}} \\ i_{qn\_\text{ref}} \end{bmatrix} = \frac{2P_{\text{ref}}}{3K} \begin{bmatrix} v_{dp} \\ v_{qp} \\ -v_{dn} \\ -v_{qn} \end{bmatrix} \tag{5}$$

where

$$K = v_{dp}^2 + v_{qp}^2 - v_{dn}^2 - v_{qn}^2 \tag{6}$$

If the load current is fed forward to the positive

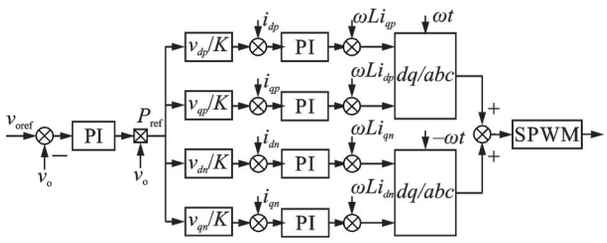

Fig.6 Output voltage control block diagram (without power feedforward)

sequence d-axis during this time, it will affect every element in the power vector due to the coupling of the voltage matrix, resulting in pulsations in the output power and limited improvement in dynamic response. To address this issue, the load current feedforward method can be enhanced. Essentially, the purpose of load current feedforward is to calculate the theoretical value of the input current based on the load current and output power. This allows the output power to be fed forward before the current reference calculation stage. Considering the feedforward link, the current reference calculation should be

$$\begin{bmatrix} i_{dp} \\ i_{qp} \\ i_{dn} \\ i_{qn} \end{bmatrix} = \begin{bmatrix} v_{dp} & v_{qp} & v_{dn} & v_{qn} \\ v_{qp} & -v_{dp} & -v_{qn} & v_{dn} \\ v_{qn} & -v_{dn} & -v_{qp} & v_{dp} \\ v_{dn} & v_{qn} & v_{dp} & v_{qp} \end{bmatrix}^{-1} \begin{bmatrix} P_{\text{ref}} + v_{\text{o}} i_{\text{o}} \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{7}$$

The control model at this time can be modified to the one shown in Fig.7.

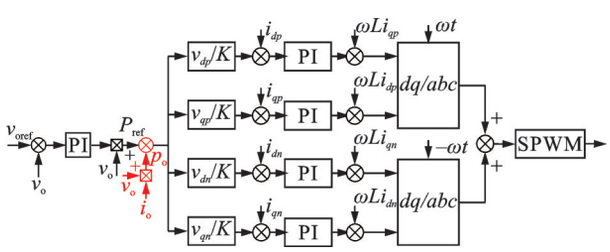

Fig.7 Output voltage control block diagram

From the model above, it is clear that the essence of this feedforward is power feedforward, ensuring the matching of input and output power to prevent excessive fluctuations in the output voltage.

According to the calculation process shown in Fig.5 of the main text, the method proposed in this paper requires a total of three multiplications, three judgments, and three subtractions. It is assumed that the DSP model used is F2812. In the F2812,

multiplication operations can usually be completed by using the hardware multiplier. When performing fixed-point multiplication using the IQMath library, generally, one multiplication operation can be completed within one clock cycle (because the F2812 has a single-cycle multiplier). The judgment operation is usually a logical comparison instruction. In the F2812, logical comparison instructions can generally also be completed within one clock cycle. The subtraction operation can also be quickly completed by using the hardware arithmetic logic unit (ALU), and generally, one subtraction operation can be executed within one clock cycle. Therefore, under normal circumstances, the increased computational load is approximately equivalent to 10 DSP clock cycles, accounting for about 0.6% of the switching cycle. Hence, the increased computational load of the method proposed in this paper is extremely low.

3 Simulation Verification

This section conducts simulation studies to verify the previous analysis, with a concise interpretation of the results. The simulation parameters are given in Table 1.

Table 1 Simulation parameters

Parameter	Value
AC voltage/V	311
AC frequency/Hz	50
Output voltage/V	750
Output power/kW	15
Switching frequency/kHz	100
Filter inductance/μH	250
DC-link capacitance/μF	800

Fig.8 shows the steady-state voltage and current waveforms under a 20% voltage drop in phase *a* at full load. At 0.06 s, the proposed zero-crossing distortion suppression method is activated, effectively mitigating the current distortion. To analyze the mechanism of distortion reduction, Fig.9 compares the modulation signals before and after applying the suppression algorithm. In Fig.9(a), significant waveform distortion is observed due to abnormal modulation and the response of the current controller. In contrast, Fig.9(b) demonstrates that by clamping the modulation signals at their respective zero-crossing points, the current can naturally cross zero without distortion. Fig.10 further presents the DC-link voltage waveforms. After the algorithm is used, the voltage ripple is significantly reduced from 2 V to approximately 0.5 V peak-to-peak, indicating improved DC-side performance.

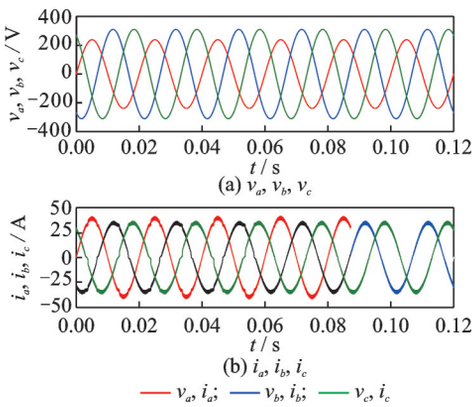

Fig.8 Steady-state input voltage and current waveforms

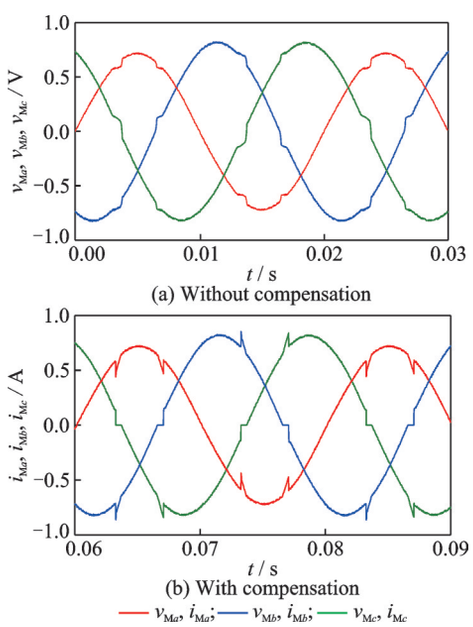

Fig.9 Steady-state modulation waveforms

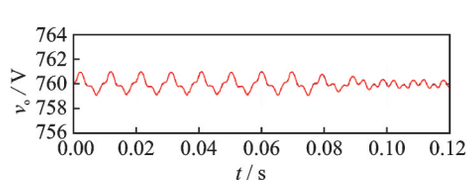

Fig.10 Steady-state output waveforms

Figs.11, 12 depict the system response to a step load decrease (from full load to half load) without using the proposed feedforward method. The current decreases slowly, resulting in a delayed reduction in input power while the load power halves abruptly. This mismatch leads to a capacitor over-

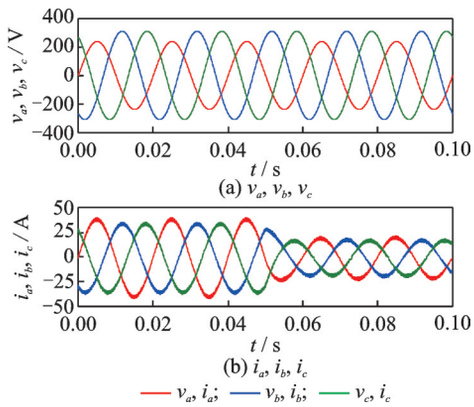

Fig.11 Full load to half load input voltage and current waveforms (without feedforward)

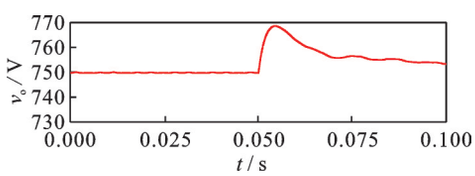

Fig.12 Full load to half load output voltage waveform (without feedforward)

charge, causing an output voltage overshoot of approximately 18 V.

In contrast, when the proposed feedforward strategy is used, the current reference is updated in real time according to power balance, enabling fast current reduction and suppressing the voltage overshoot. The corresponding waveforms are shown in Figs.13,14, where the output voltage ripple is limited to around 5 V.

Fig.15 illustrates the three-phase current and modulation waveforms under extreme imbalance, with a 60% voltage drop in phase A. Before 0.46 s, no suppression is applied, and the current is severely distorted. After 0.46 s, the zero-crossing suppression method is enabled. Although slight overmodulation occurs due to the imbalance, the current quality improves significantly, and the distortion is largely eliminated.

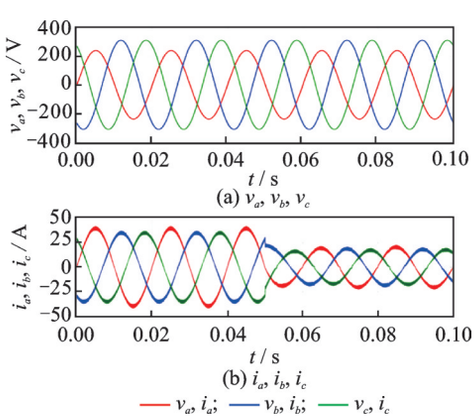

Fig.13 Full load to half load input voltage and current waveforms (with feedforward)

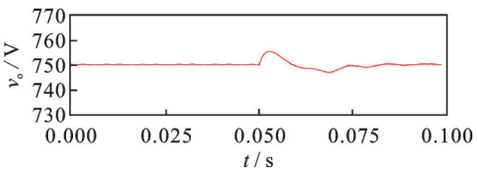

Fig.14 Full load to half load output voltage waveform (with feedforward)

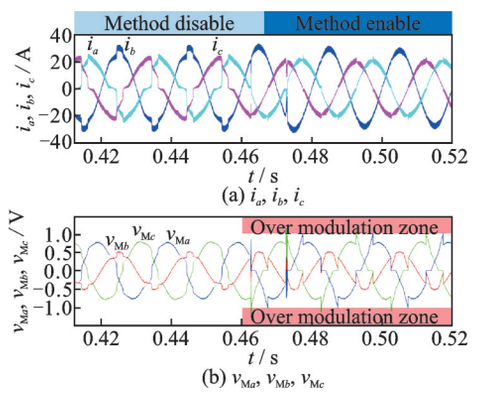

Fig.15 Three-phase currents and modulation waves under 60% voltage sag in phase a

To further verify the method under different degrees of imbalance, Fig.16 presents the simulation result for a 40% voltage drop in phase a. The method remains effective as long as excessive overmodulation is avoided.

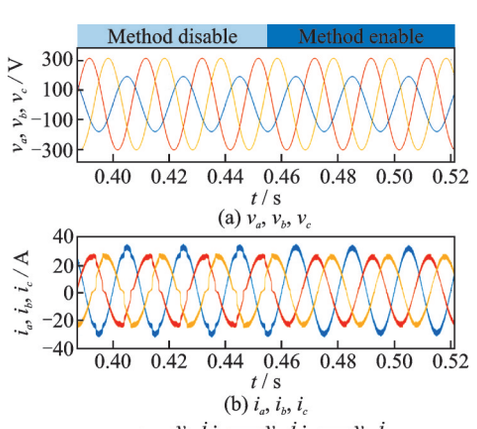

Fig.16 Waveforms under 40% voltage sag in phase a

To evaluate the robustness of the proposed feedforward method under various load types, a pulsed load is simulated, where the output power repeatedly jumps between half and full load. As shown in Fig.17, the output voltage maintains good

quality, confirming the effectiveness of the method regardless of load variation, where V_{pp} means the peak to peak value of voltage.

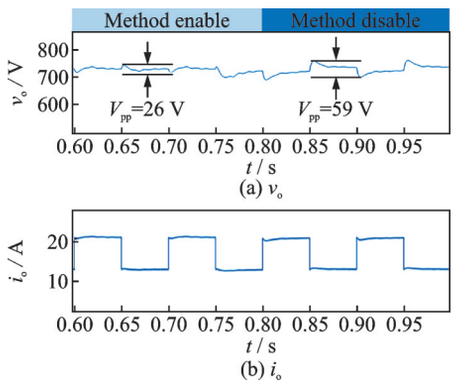

Fig.17 Output voltage waveform under pulsed load

Finally, the influence of the proposed method on the system power factor is evaluated based on the definition in IEEE Std 1459—2010. According to the standard, the power factor under unbalanced conditions is defined as the ratio of total active power to total apparent power. The simulation is re-run accordingly, and the resulting power factor trajectory is shown in Fig.18.

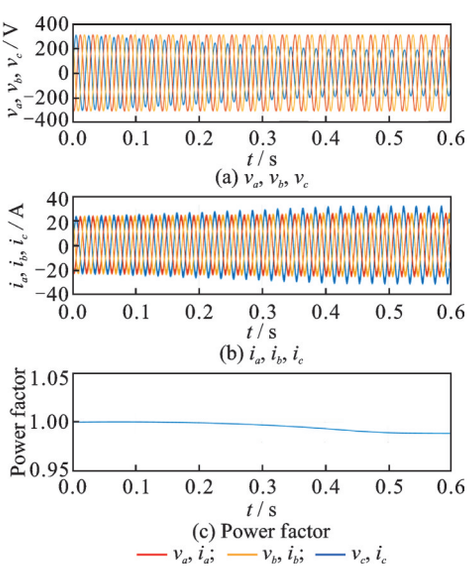

Fig.18 Power factor wave with voltage sag

4 Experimental Verification

To verify the correctness of the theoretical analysis presented earlier, a hardware-in-the-loop (HIL) verification platform was built and relevant experiments were conducted. In the hardware-in-the-loop experiment, the power circuit is calculated in real-time in the real-time simulator, and the voltage and current information is output to the controller for control. This enables rapid verification of the correctness and effectiveness of the control method. Fig.19 shows the basic structure of the experimental platform. The main power circuit model is built using a laptop and downloaded to the simulator, and the control program is written and downloaded to

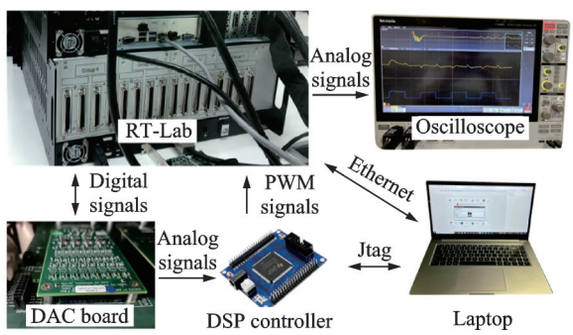

Fig.19 Hardware in the loop experimental platform structure diagram

the DSP for control. The DSP collects the analog signals output by the simulator through the digital-to-analog conversion board and outputs PWM signals to the simulator to complete the closed-loop control, and the simulation waveforms are observed through an oscilloscope.

For the zero-crossing distortion compensation algorithm proposed in this paper, Figs.20,21 respectively present the experimental results when the phase a voltage drops by 20% and 40%. The algorithm proposed in this paper is enabled at the intermediate moment, and it can be seen that the zero-crossing distortion is well suppressed. Meanwhile, Fig.22 also presents the waveforms of the output voltage before and after the algorithm is enabled. It can be seen that the output voltage ripple becomes smaller after the algorithm proposed in this paper is enabled.

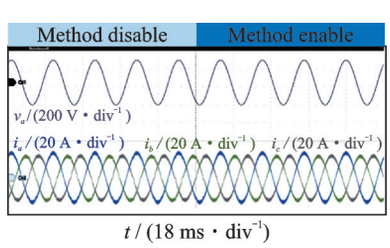

Fig.20 Experimental waveform of 20% voltage sag in phase a

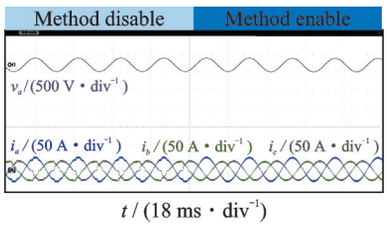

Fig.21 Experimental waveform of 40% voltage sag in phase *a*

For the dynamic performance optimization method proposed in this paper, Figs.23, 24 respectively present the output voltage waveforms during load shedding. Among them, Fig.23 does not use the method proposed in this paper, while Fig.24 uses the method proposed in this paper to achieve a smaller voltage ripple. To prove the adaptability of the method proposed in this paper to pulsed loads such as radar, Fig.25 presents the waveforms of the output voltage v_o and output current i_o under different pulsed load conditions. The algorithm proposed in this paper is enabled at the intermediate moment, which can effectively achieve the stable control of the output voltage.

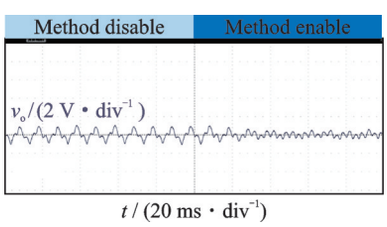

Fig.22 Output voltage waveform comparison before and after enabling zero-crossing distortion compensation algorithm

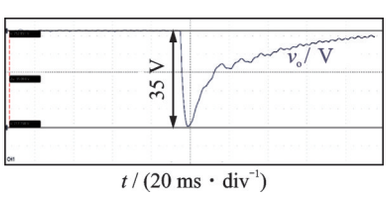

Fig.23 Output voltage waveform without proposed method

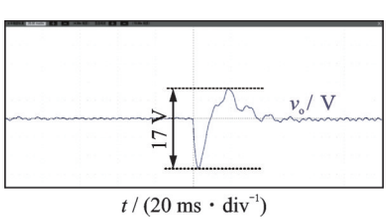

Fig.24 Output voltage waveform with proposed method

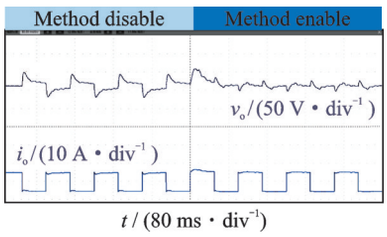

Fig.25 Output voltage and current waveforms

5 Conclusions

This paper thoroughly analyzes the distortion issues and load current feedforward challenges faced by the Vienna rectifier under unbalanced three-phase voltage conditions. It identifies that the primary cause of current distortion is the phase discrepancy between the current reference and the grid voltage, leading to significant modulation errors. To address these issues, a novel and straightforward compensation method is proposed to mitigate these distortions. Furthermore, the paper critically evaluates the limitations of traditional load current feedforward techniques under unbalanced voltage conditions and explains their ineffectiveness. Building on the principle of power conservation, an improved feedforward approach is introduced, which enhances the system's dynamic performance under unbalanced conditions. To validate the proposed compensation and feedforward methods, extensive simulation analyses are conducted. The simulation results demonstrate that the new approach significantly reduces distortion, improves load current response, and optimizes overall system performance, effectively addressing the challenges posed by three-phase voltage imbalance.

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Author contributions Mr. **HUANG Xiaoqi** conducted the theoretical analysis, wrote the manuscript, and performed the experimental verification. Mr. **MA Yaopeng** and Mr. **BEN Guixin** contributed to build the RT-Lab testbench. Dr. **LIU Chengzi** provided guidance and suggestions for both the manuscript writing and experimental work. All authors commented on the manuscript draft and approved the submission.

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不平衡电网下Vienna整流器的优化控制方法

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摘要:维也纳整流器因其效率高且设计简洁,成为高功率整流领域的广泛采用方案。然而,在三相电压不平衡条件下,其性能会下降,导致电流过零畸变和动态响应恶化。本文探究了这些畸变的成因,确定输入电流与电网电压之间的相移为主要因素,并提出了一种有效的畸变相位识别策略,引入了通过改进电流参考计算和优化功率前馈策略来提升动态性能的方法。该方案优化了系统对负载变化的响应,并在不平衡条件下维持输出电压稳定性。仿真结果验证了所提方法在降低电流畸变和改善整体性能方面的有效性。

关键词:过零畸变;三相不平衡;整流器;功率前馈